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ELECTRONIC DESIGN

18 APR 1994

FEBRUARY 7, 1994

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- HARNESSING MULTIPROCESSING FOR DSP SYSTEMS
- COMPUTERS/EMBEDDED SYSTEMS SECTION
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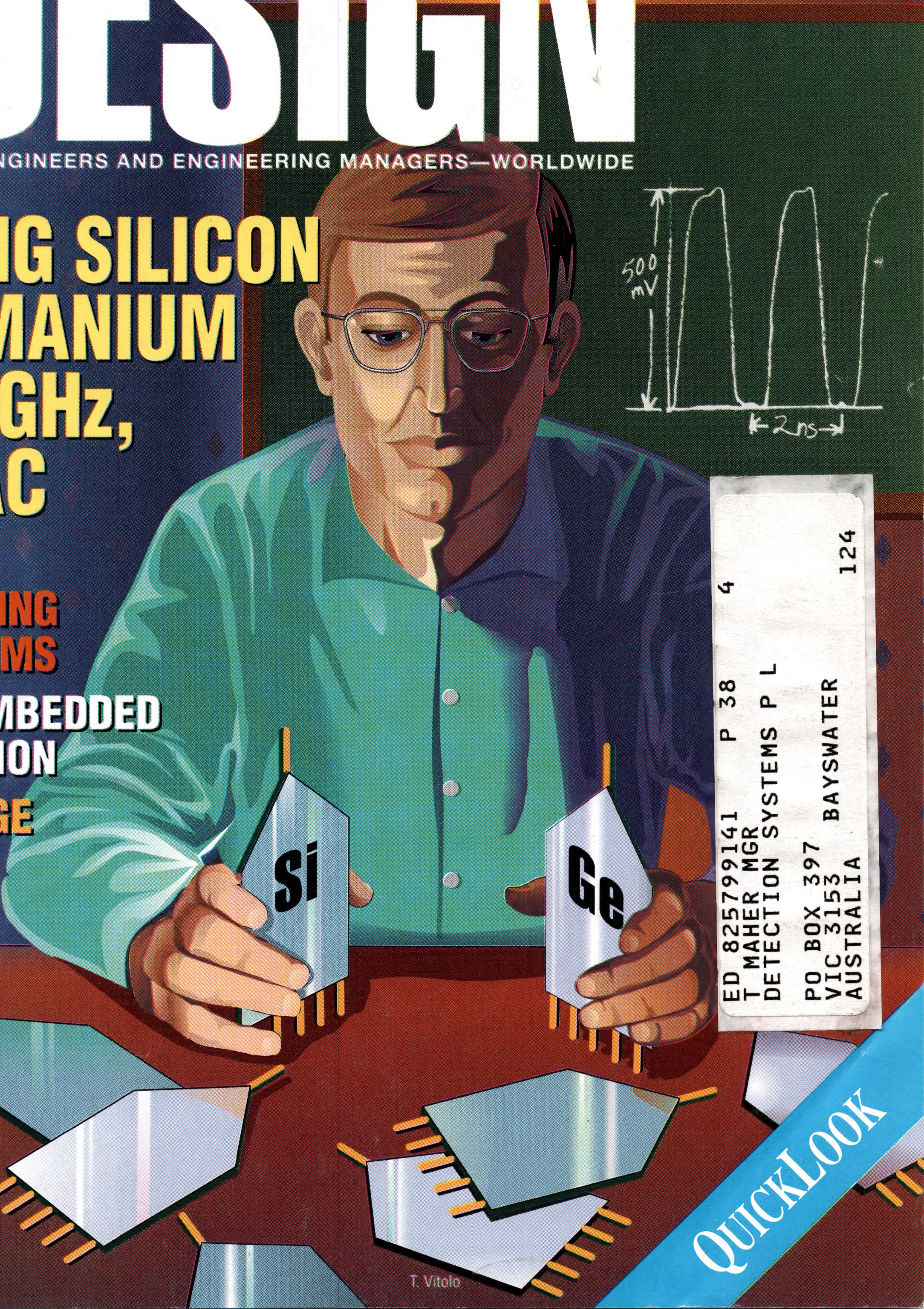

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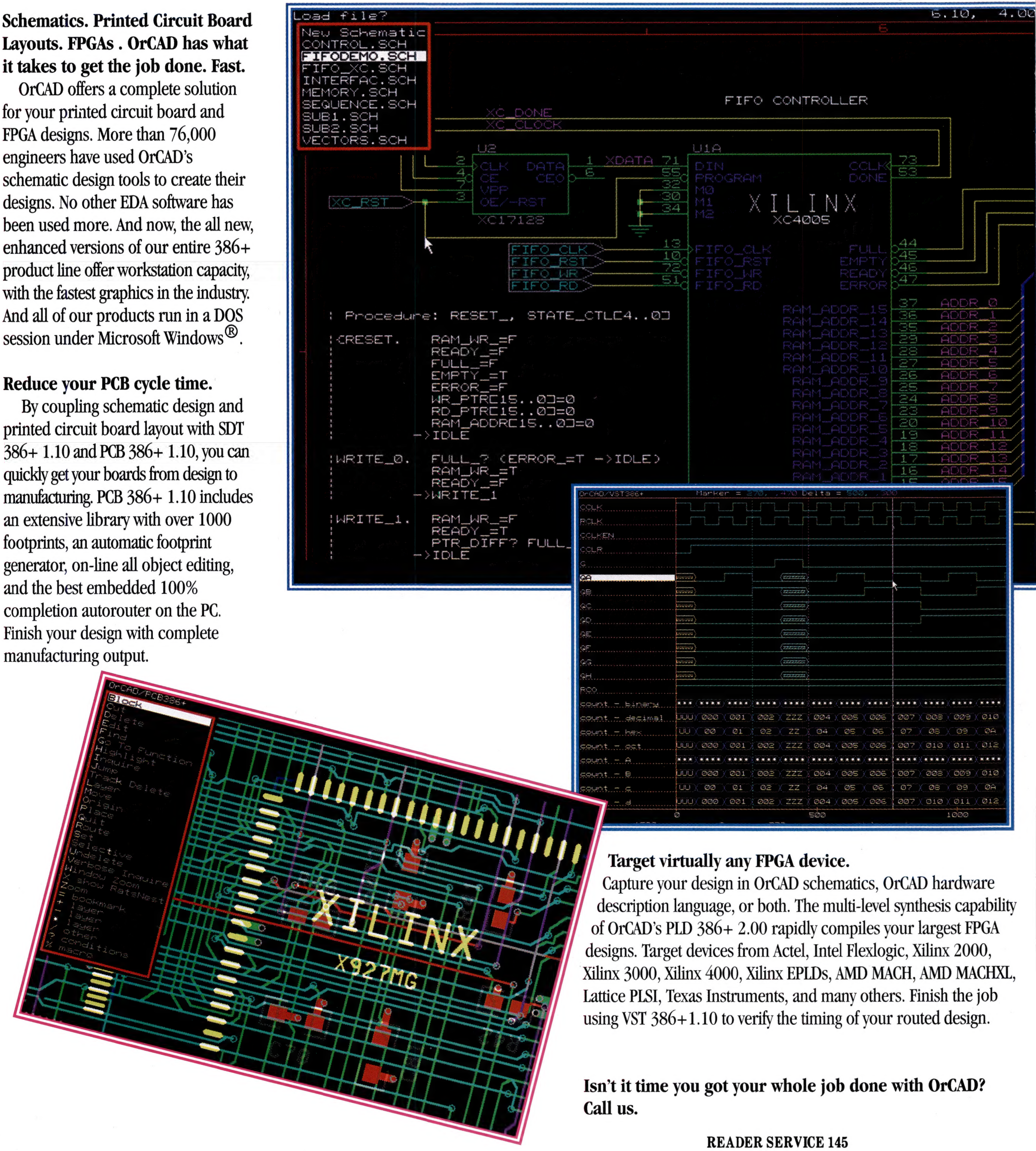

```
; Procedure: RESET_, STATE_CTL[4..0]

;<RESET.        RAM_WR_=F
;               READY_=F
;               FULL_=F
;               EMPTY_=T
;               ERROR_=F
;               WR_PTR[15..0]=0
;               RD_PTR[15..0]=0
;               RAM_ADDR[15..0]=0
;             ->IDLE

;WRITE_0.       FULL_? (ERROR_=T ->IDLE)
;               RAM_WR_=T
;               READY_=F
;             ->WRITE_1

;WRITE_1.       RAM_WR_=F
;               READY_=T
;               PTR_DIFF? FULL_
;             ->IDLE
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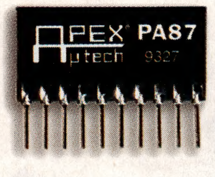

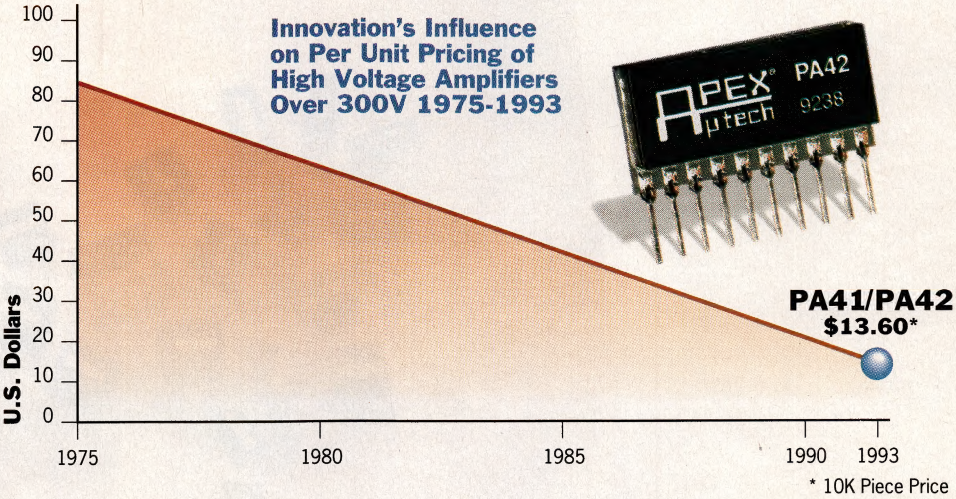

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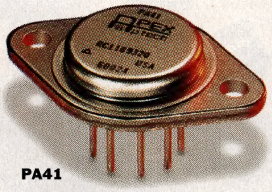

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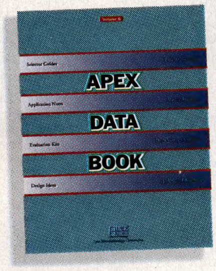

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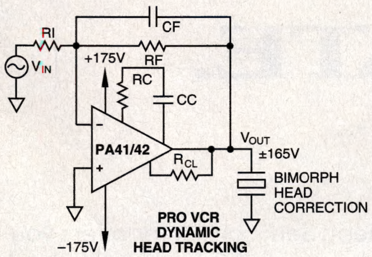

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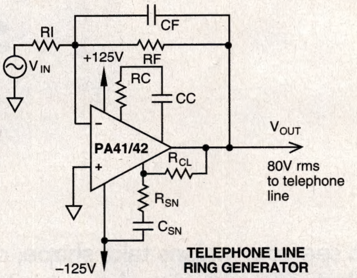

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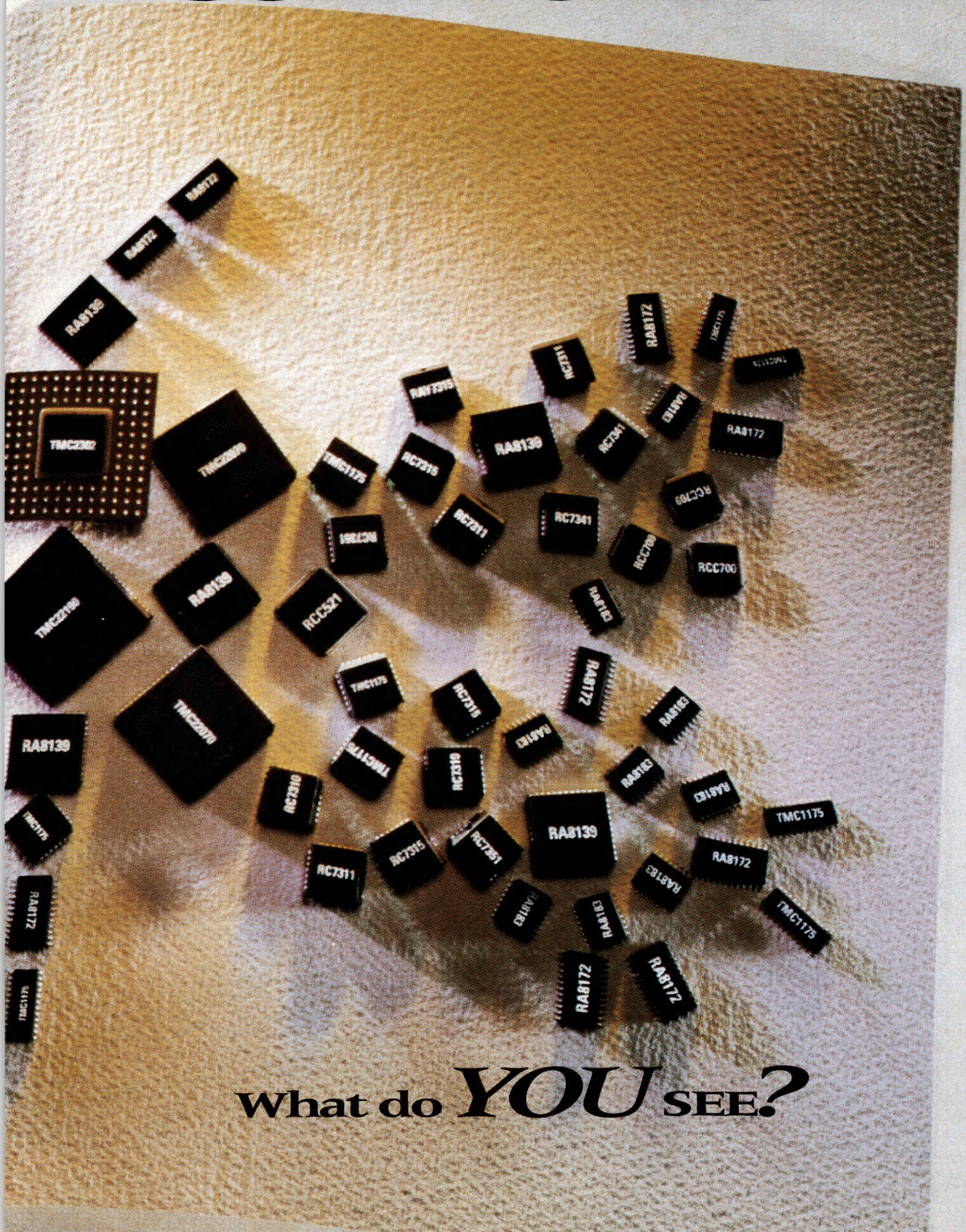

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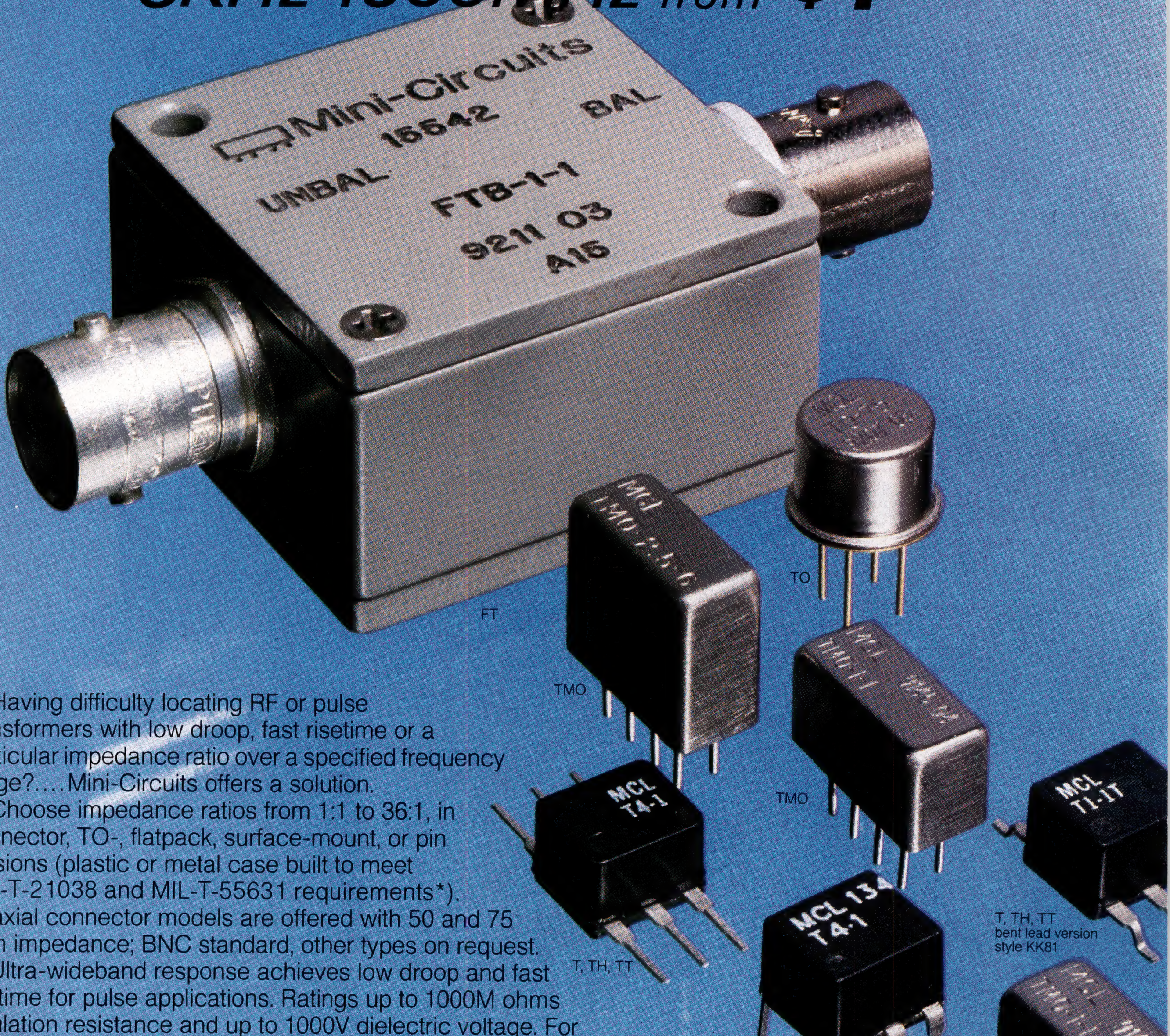

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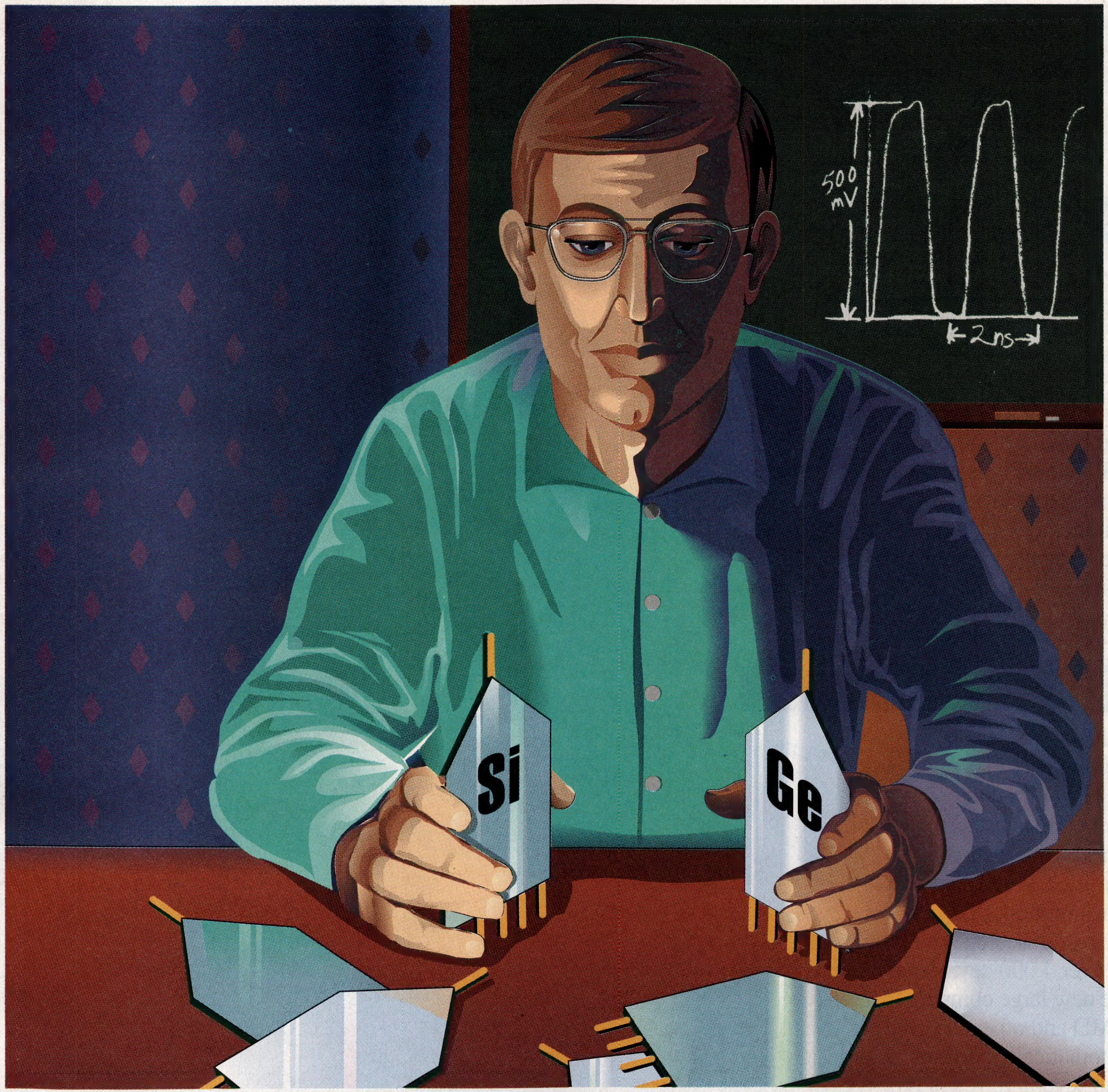

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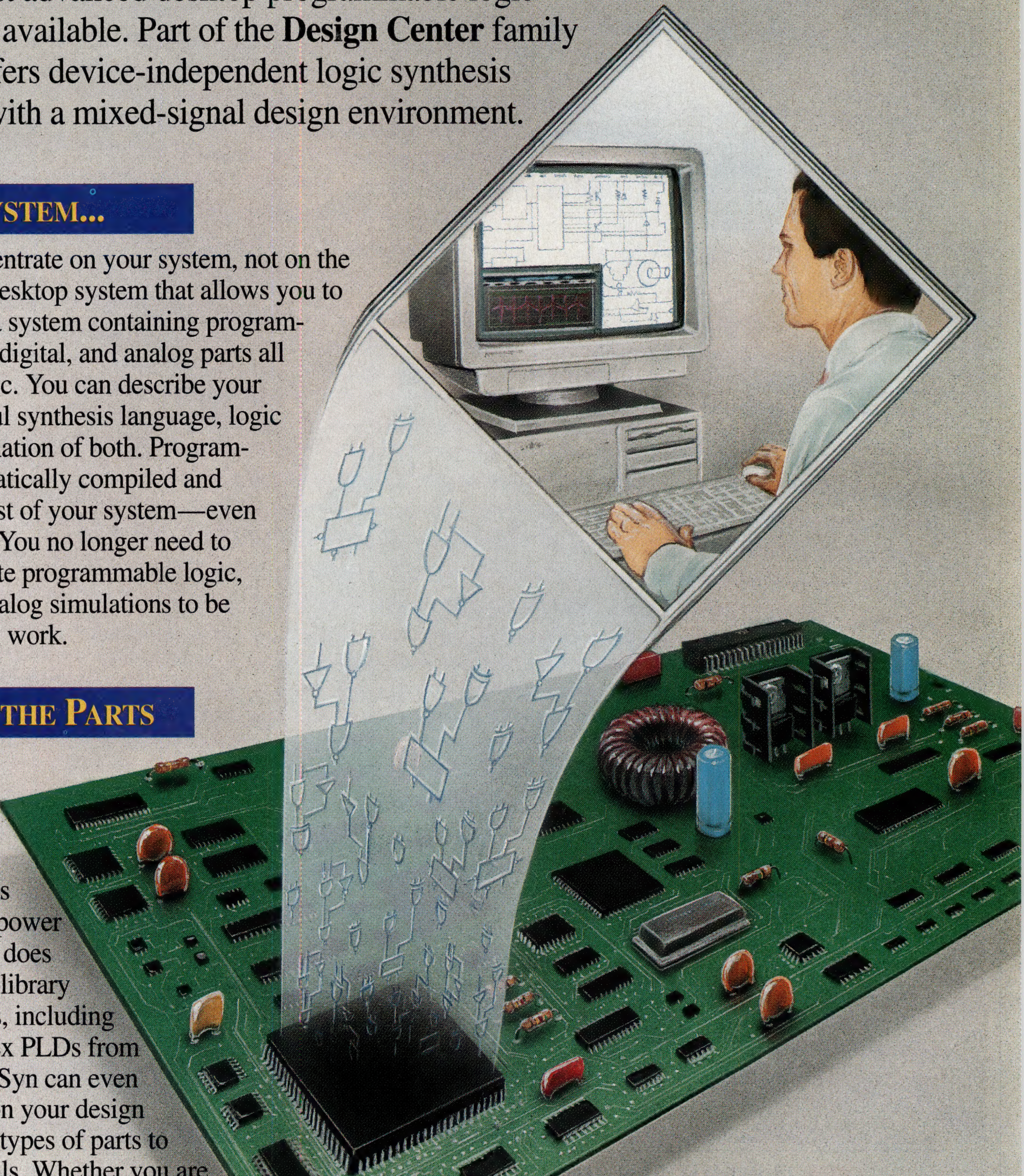

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These oscillators were among the highest quality made during the 1950s, and were a fixture in most industrial and university labs. The slow-motion-drive dial should recall a tactile memory for many engineers—the tuning mechanism had an extremely smooth feel as you rotated it through the band.—SS

Valley Community TV Systems

A paper presented at the Winter General Meeting of the AIEE investigated one of the major problems of Community TV System design and the choice of suitable amplifiers for relaying signals along the main trunk line. In the paper, entitled "Line Amplifiers for Community Television Systems," by K. A. Simons, D. Kirk, and H. J. Arbeiter of the Jerrold Electronics Corp. (Philadelphia, Pa.), the growth of Community TV Systems together with resulting techniques and developments was discussed. Although some of the art is entirely new, the basic technique of moving television frequency signals efficiently from one place to another is closely allied with long-distance telephony.

The possibility of a Community Television System exists where there is a large group of people who cannot receive satisfactory signals directly, located within a few miles of a site where satisfactory reception is possible. The most obvious case is a valley town shadowed by a mountain. The system operator installs high-gain antennas and sensitive receiving equipment on top of the mountain where the signals are relatively strong and distributes them, via coaxial cable, to the homes in the town. Since these signals must be delivered to the customers on the standard television channels between 54 and 216 Mc, present practice is to select channels most suitable for the system, and convert the frequencies of the received signals where necessary to fit this pattern. Although adjacent channel operation is possible, it has not been widely used because of the difficulties of preventing interference between channels, and it will not be considered. The paper considers three important possibilities: (1) Separating channels frequency-wise at each repeater point and amplifying each with a separate single-channel cascade amplifier; (2) Separating channels into two groups and amplifying those between 2 and 6 with one broad-band cascade amplifier, and those between 7 and 13 with another; and (3) Using a single distributed amplifier for all channels.*(Electronic Design, February 1954, p. 8.)*

Cable TV was just getting off the ground when this paper was presented at the annual meeting of the AIEE (which later merged with the Institute of Radio Engineers to form the IEEE). This article makes a couple of interesting points: the similarities with telephony and the limited number of channels. Today, cable TV and telephone companies are gearing up for head-to-head competition while the number of available channels is far beyond what was envisioned when the first cable-TV operators erected that antenna on a hilltop.—SS

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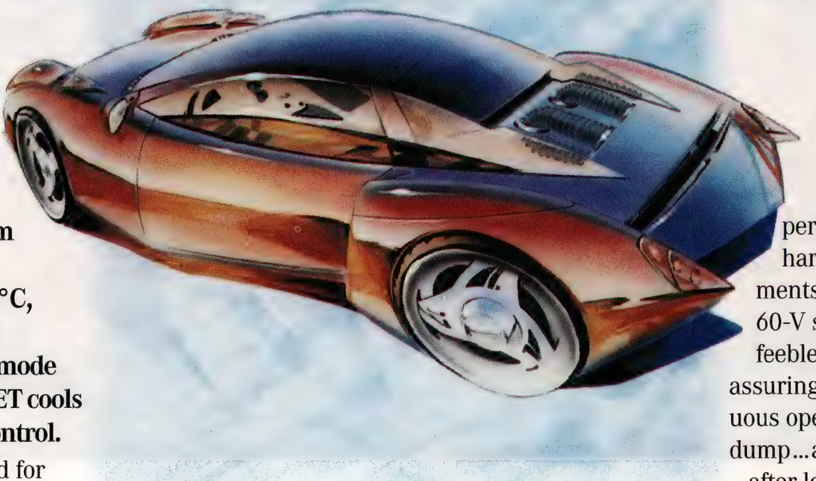

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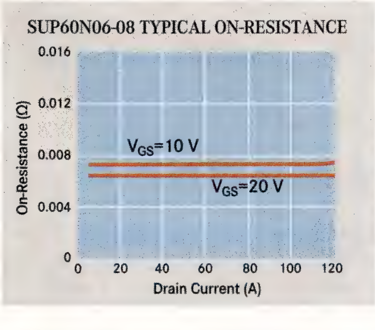

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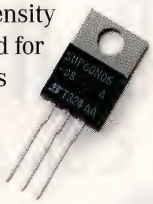
The rugged SUP60N06-08, with its guaranteed 8-mΩ maximum on-resistance and 175°C maximum junction temperature, will reduce power dissipation and enhance performance in the harshest of environments. This is a robust 60-V solution, not a feeble 50-V product, assuring you of continuous operation, load dump...after load dump ...after load dump.

Unparalleled part count reduction.



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Create cooler car electronics.

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PORTABLE POWER

The Competitive Edge of the Low Voltage 68HC11

Low-voltage 68HC11 microcontrollers from Motorola put you on the path to low-power portability, without putting the brakes on performance. With extensive on-chip integration — including A/D converters and EEPROM — and efficient low-voltage operation, these microcontrollers provide the high performance and low power consumption your portable applications need to run stronger, longer.

No Pain, No Drain. Building on the industry-standard 68HC11 architecture, our low-voltage derivatives push battery drain problems out of your way, freeing you to pull ahead of the pack. So you can stay on the fast track to cost-efficient, low-power, high-performance solutions for your portable applications.

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Everyone's a Winner. Put the M68EBLP11KIT to the test. Complete the projects included with the kit, and send in your results. We'll send you a valuable gift commemorating your completion of our 68HC11 low-power training course. Plus, enter our "Portable Power" Design Contest and qualify to win one of eleven $511 cash prizes and a chance to have your low-power design technique published by Motorola.

For details, contact your Motorola sales office or Motorola authorized distributor, or fax your inquiry to (800) 347-6686.

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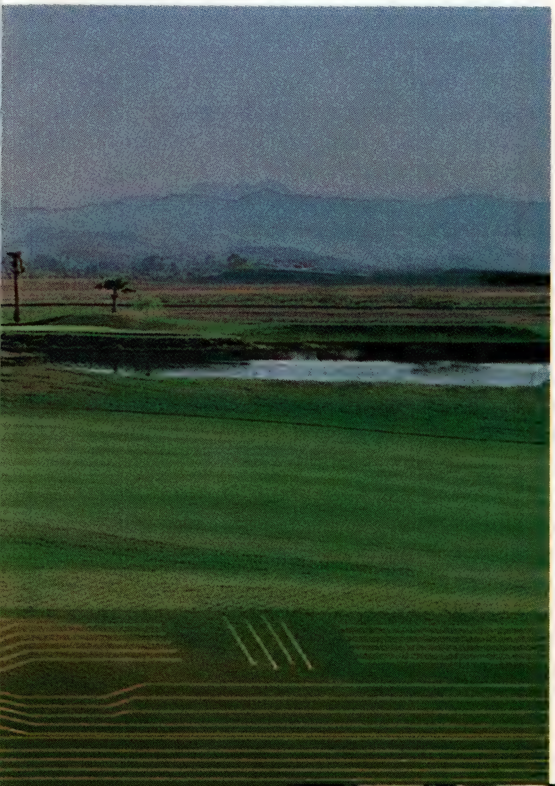
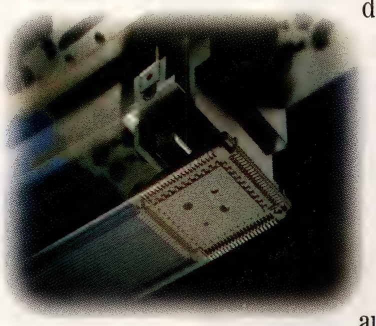
How to stay out of the rough in surface mount technology.

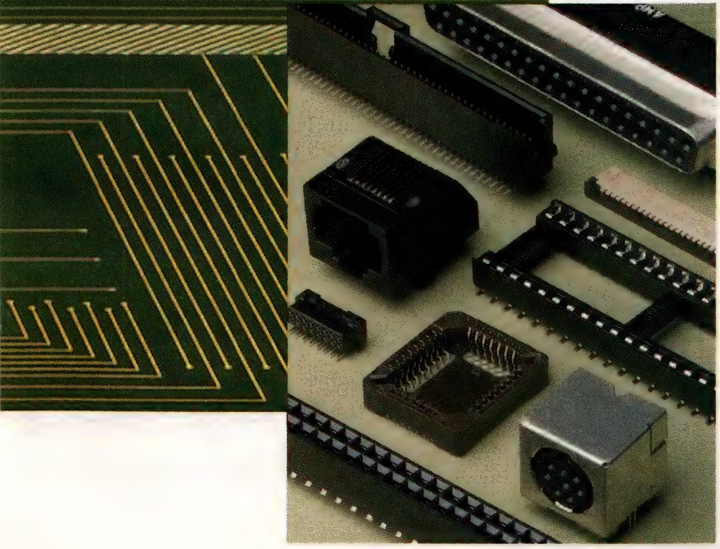


Surface mount interconnects are a whole new game in technology. And as in most new games, a little help from the pros makes life easier.



Each surface mount application presents its own problems requiring a unique solution. Our experience in design and manufacturing can help guide you through the options, giving you a clearer understanding of what you can (and can't) do to integrate surface mount interconnects into existing or new products.

We'll show you the variations in form you can choose from — from through-hole compatibles to new, ultra-fine-pitch SMT products. We'll make sure the contact configuration and foot design you choose are right for the physical requirements of your system. We'll help determine optimum holddown type, based on how your product will be assembled and used. And we'll show you how the right combination can answer design needs and fit successfully into production.



We offer the manufacturing technology you need, too: our products are designed for either automated pick-and-place or robotic application. They're available in tape and reel packages (including EIA-481), tubes, and trays to meet manufacturing requirements. In fact, the packaging, tooling, and feeder modules we offer can all be tailored to your unique assembly environment.

Want more help? We'll also move you ahead in your design efforts, keep you up-to-the-minute on new advances, and simplify your design process. Full technical information, catalog sheets, and 2D and 3D models of many product lines are available in CD-ROM format to shorten your design cycle.

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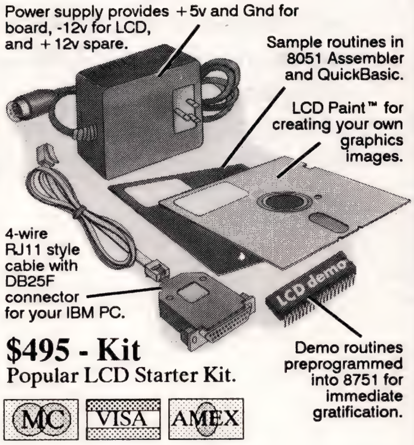
240 x 64 pixel Supertwist LCD mounts directly onto CYB003 proto-typing board.
Kit provides serial interface to IBM PC for quick prototyping. Board also supports displays up to 240 x 128 pixels.
Interface to 6 soft keys or 4 x 4 key matrix.
Dial 0-25k ohms for LCD contrast.
CY325 LCD CONTROLLER
* The CY325 LCD Windows Controller provides parallel or serial high-level control of Instrument-size LCDs. Up to 256 built-in windows support window-relative text, bargraphs, waveforms, and plots. Text and graphics are maintained in separate planes, facilitating special effects. Complete User Manual included.
Wirewrap area for custom circuitry or backlight.
RJ 11 serial jack for RxD, TxD, CTS, and GND, plus 2 spares.
5 Pin Power DIN.
Alternate Power Connector.
Add your own 8051 CPU for stand alone operation.

Kit also includes:


Power supply provides +5v and Gnd for board, -12v for LCD, and +12v spare.
Sample routines in 8051 Assembler and QuickBasic.
LCD Paint™ for creating your own graphics images.
4-wire RJ11 style cable with DB25F connector for your IBM PC.
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Demo routines preprogrammed into 8751 for immediate gratification.

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READER SERVICE 165

THE PORTABLE WORLD

Power and size: Those are usually the two key design parameters electronics engineers consider when the topic is portable electronics systems. Specifically, that means minimizing the battery power drain and packing lots of electronics, display, and input devices into a small package. But that's only a fraction of what's involved in designing portable electronic systems. Designers also have to create a rugged unit that can handle both external and internal RFI, select and efficiently drive the display, get the right input device ergonomics that match the application, and accommodate a host of other design restrictions. It could, in fact, be argued that portable electronic systems—computers, communicators, medical monitors, whatever—represent the ultimate in design challenges, which must be solved under severe time-to-market pressures.

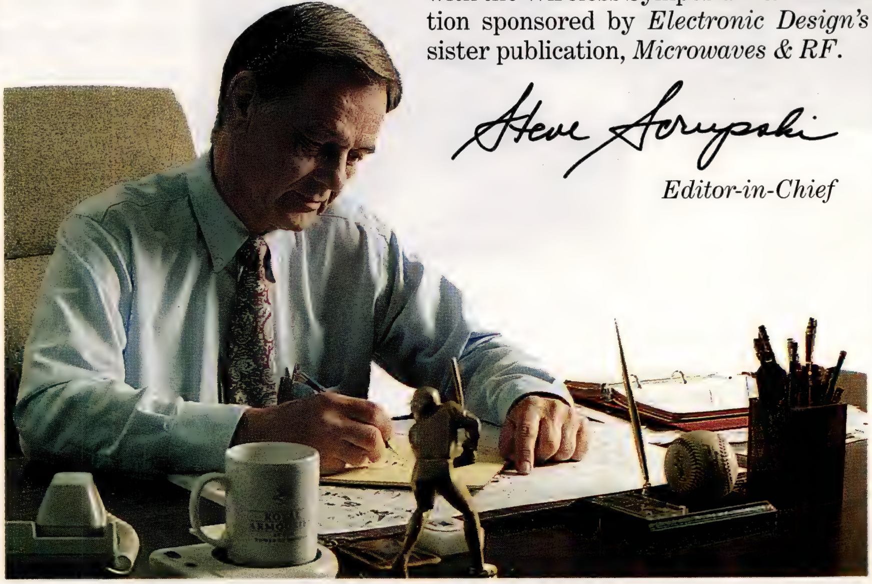
This topic comes to mind because next week, *Electronic Design* will be sponsoring the Portable by Design conference at the Santa Clara Convention Center. Upon reviewing the conference technical program put together by chairman Jack Shandle, *Electronic Design's* Advanced Technology Editor, it becomes clear that portable electronics design is a different animal from most other types of equipment design. What makes it even more intriguing are the strong market indicators of growth among all types of portable systems.

The market acceptance and resultant increasing demand for portable electronics gear will offer new opportunities for electronics designers. One basic but crucial skill designers will have to sharpen is their ability to work as a design-team member. The much talked about (in some cases, perhaps too much) concept of concurrent engineering appears to be a necessity in the design of this type of equipment. To a much higher degree than in other types of systems, the design problems involve the interaction between electronic and mechanical constraints—placement of components, heat dissipation, user-friendly features, ruggedness, attractive packaging. These combined with time-to-market goals seem to call for a team approach to the design. Getting a product out the door in a reasonable time is possible only if the EEs and MEs work simultaneously in solving the long list of problems.

This interplay between mechanical, ergonomic, and electronic functionality is mirrored in the technical program of the Portable by Design conference. The conference, which will be held Feb. 14-18, will bring together top experts in the industry, presenting workshops and technical papers on every major aspect of designing portable electronics equipment. The conference runs simultaneously with the Wireless Symposium & Exhibition sponsored by *Electronic Design's* sister publication, *Microwaves & RF*.

Steve Scrypski

Editor-in-Chief



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Available with LO drive levels from +7 to +17dBm, performance features include very low conversion loss flat over the entire band, high isolation (L-R, L-I), and well-matched VSWR at all ports.

All-welded internal and external construction is used to assemble and package the TUF-unit in its tiny 0.5 by 0.2 by 0.25 in. metal case, for plug-in or surface-mount* assembly.

TUF-Ultra-Rel™ mixers are guaranteed for five years and boast unprecedented "skinny" sigma (δ) unit-to-unit repeatability as shown in the Table.

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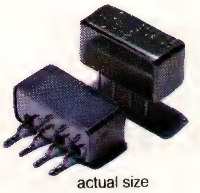

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SPECIFICATIONS

Model	LO Power (dBm)	Freq. LO/RF (MHz)	■ Conv. Loss (dB)		Isol. L-R (dB)	Price,$ Ea. 10 qty
			$\overline{X}$	δ		
TUF-3	7	0.15-400	4.98	0.34	46	5.95
TUF-3LH	10		4.8	0.37	51	7.95
TUF-3MH	13		5.0	0.33	46	8.95
TUF-3H	17		5.0	0.33	50	10.95
TUF-1	7	2-600	5.82	0.19	42	3.95
TUF-1LH	10		6.0	0.17	50	5.95
TUF-1MH	13		6.3	0.12	50	6.95
TUF-1H	17		5.9	0.18	50	8.95
TUF-2	7	50-1000	5.73	0.30	47	4.95
TUF-2LH	10		5.2	0.3	44	6.95
TUF-2MH	13		6.0	0.25	47	7.95
TUF-2H	17		6.2	0.22	47	9..95
TUF-5	7	20-1500	6.58	0.40	42	8.95
TUF-5LH	10		6.9	0.27	42	10.95
TUF-5MH	13		7.0	0.25	41	11.95
TUF-5H	17		7.5	0.17	50	13.95
TUF-860	7	860-1050	6.2	0.37	35	8.95
TUF-860LH	10		6.3	0.27	35	10.95
TUF-860MH	13		6.8	0.32	35	11.95
TUF-860H	17		6.8	0.31	38	13.95
TUF-11A	7	1400-1900	6.83	0.30	33	14.95
TUF-11ALH	10		7.0	0.20	36	16.95
TUF-11AMH	13		7.4	0.20	33	17.95
TUF-11AH	17		7.3	0.28	35	19.95

*To specify surface-mount models, add SM after P/N shown.

■ $\overline{X}$ = Average conversion loss at upper end of midband ($f_u/2$)
δ = Sigma or standard deviation

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F 145 REV.G

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[*Because its* **FAST PAGE MODE** *is so rapid.*]

The new 4-meg VRAM doesn't just give you the most memory any VRAM ever has. If it's a Samsung part, it also gives you the highest *performance* any VRAM ever has.

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PART	ORG.	SPEED
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KM428C257	256K x 8	60ns
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KM424C257	256K x 4	60ns

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A *Generation* AHEAD.

TECHNOLOGY BRIEFING

HIGH-SPEED CLOCKING PUSHES CMOS

As clock speeds continue to climb in microprocessors and communications systems, it's getting more difficult to generate the clock signals that control the timing while minimizing clock skew. At next week's International Solid State Circuits Conference in San Francisco, an unprecedented number of papers will detail advanced timing and data-recovery circuits as well as high-performance logic implementations. These papers, in Sessions 6 and 18, will show designers just how far CMOS and bipolar technologies can be pushed to implement high-performance systems.

High-speed data-communications applications, such as the 125-Mbit/s FDDI standard, demand both low-cost and high-performance circuits. To achieve that, designers at Advanced Micro Devices Inc., Sunnyvale, Calif., were able to get by with a 0.8-µm CMOS process thanks to a proprietary, synchronous uniform sampling scheme and an edge-position averaging algorithm. The resulting digital phase-locked loop, discussed in Session 6, allows systems to recover binary data at rates from 75 to 230 Mbits/s.

DAVE BURSKY
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In another paper, the Information Systems Laboratory at Stanford University proposes that phase-modulation techniques be used to move multiple bits over each pin within each clock cycle, rather than push the clock frequency beyond the range CMOS can comfortably handle. The scheme does this by using both rising and falling edges of a 20-MHz clock signal. On-chip PLLs ensure that drivers and receivers have equal delays.

Bipolar transistors are behind a 156-MHz PLL-based clock and data-recovery circuit and an 8-GHz clock-recovery and data-regenerator to be described by Nippon Telegraph and Telephone Public Corp., Atsugi, Japan, and Ruhr Universitat, Bochum, Germany, respectively. NTT's PLL makes novel use of a sample-and-hold scheme to ensure stable operation. When tested with a pseudo-random bit sequence $2^{23}-1$ bits long, the chip showed an rms data pattern jitter of just 1.2°. Ruhr's researchers designed a 2-to-9-GHz quadrature VCO based on a modified ring oscillator. The oscillator is used with a master-slave D flip-flop and a phase-and-frequency locked loop. The combination can perform data regeneration at rates of 8 Gbits/s with the on-chip VCO and up to 15 Gbits/s with an off-chip VCO.

Designers at AT&T Bell Laboratories, Holmdel, N.J., and Allentown, Pa., pushed biCMOS technology to its limit by crafting a 6-GHz PLL that consumes just 60 mW when operated with a 2-V supply. The PLL has an rms jitter of just 3.1 ps at 6 GHz and requires an active chip area of just 500 by 500 microns.

Pushing the current limits of GaAs quantum-well high-electron-mobility transistors, researchers at the Fraunhofer Institute for Applied Solid-State Physics, Freiburg, Germany, will detail a 0.3-µm, HEMT-based, 19-GHz, clock-recovery circuit. The circuit employs a digital phase-locked loop that includes a VCO with a center frequency of 18.35 GHz and a tuning range greater than 2 GHz for applications in high-speed optical networks and test systems.

High-speed operation also will be the focus of presentations in Session 18. For instance, Intergraph, Palo Alto, Calif., will detail a novel regenerative push-pull differential logic family. Thanks to this development, circuits will be able to perform complex Boolean functions with propagation delays just one-third that of other differential logic schemes, and up to 40% faster than dynamic logic implementations. In one example, a 64-bit adder implemented in a 0.7-µm 3-V process yielded a delay of just 1.5 ns. Additional presentations from Intel Israel Ltd., Haifa, and a combined effort by Rambus Inc., Mountain View, Calif., and NEC Corp., Kanagawa, Japan, will detail delay-locked loops that help deskew clock edges and deliver clocks that run at speeds of up to 104 MHz and 500 MHz, respectively. Copies of the conference proceedings and slide supplements can be ordered through the IEEE, Palo Alto, Calif. Call (415) 327-6622.

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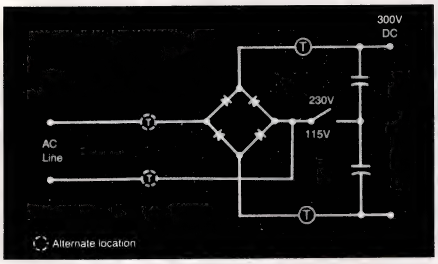

Keystone has designed special disc-style NTC thermistors with crossed leads in 20 types with "cold" resistance values @ 25° C from 0.5 to 120 ohms. A Designer's Kit with one each of 20 different types is available.

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Conserve Energy.

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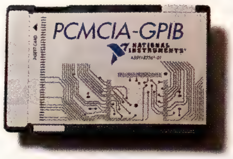

You don't have to worry about wasting any energy developing new application programs for your portable system. Your existing NI-488.2™ programs written for the industry-standard AT-GPIB, GPIB-PCII/IIA, or any of our IEEE 488.2 hardware, will be ready to run.

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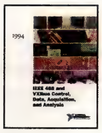

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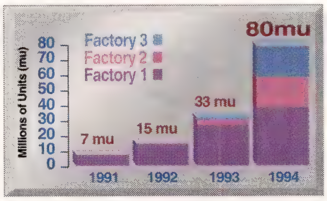
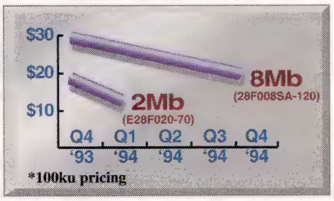

Intel Flash Memory Factory Output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*100ku pricing

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SHARP

PROGRESS REPORT

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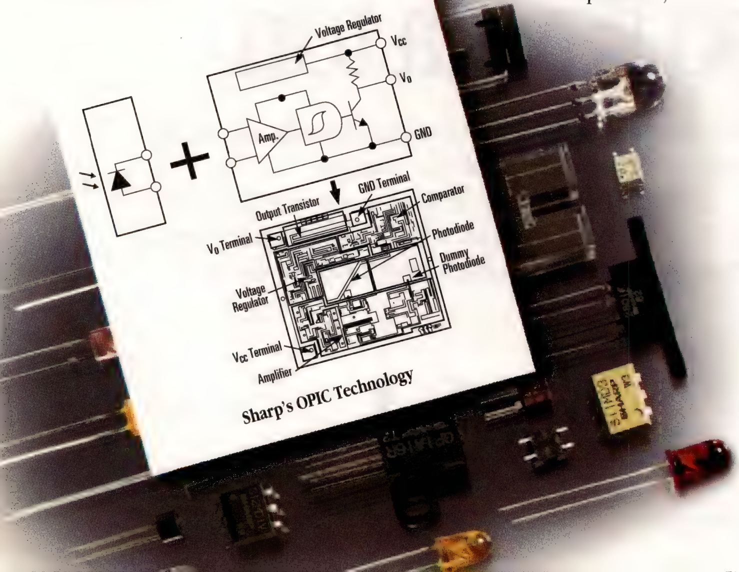
Twenty-five years ago, Sharp introduced the gallium arsenide LED: the heart of the photocouplers and photointerrupters that are the ubiquitous electrical isolators and switching components of industrial control systems.

Sharp photocouplers protect sensitive circuitry from high voltage machines. They give you 1000 times the switching speed of mechanical isolators, plus lower power consumption, smaller size, longer life, and better shielding from noise. And compared to other optoelectronic components,

With three decades of opto technology behind it, Sharp has pushed device functionality to new extremes. Sharp's proprietary Optical IC (OPIC) process technology combines photodiodes and their peripheral circuitry on a single chip to achieve new dimensions in device miniaturization. In addition, you are assured of better isolation voltage and the highest reliability via Sharp's packaging innovations like its patented double-transfer-mold process.



Sharp's OPIC Technology

From early light to the latest

Sharp's opto is well-known for three critical advantages:

RELIABILITY. CAPABILITY. AND CHOICE.

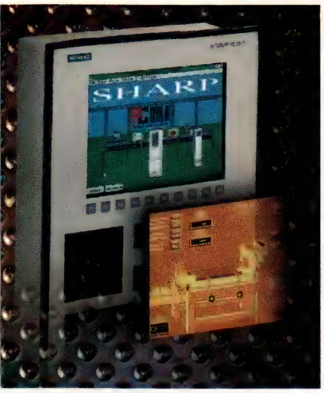
One faulty photocoupler can be the weak link that paralyzes a production line. Your best hedge against this is the added voltage isolation protection afforded by Sharp's patented double-transfer-mold technology. Sharp uses two separate molds of epoxy resin as part of a process that promises higher isolation voltage, tighter tolerances and more reliable performance even as the size of photocouplers keeps shrinking.

And when it comes to putting the most opto capability on the least real estate, you can turn to Sharp's Optical Integrated Circuit (OPIC) technology. We offer more than 50 ways to

One of Sharp's broad range of CCDs can be the ideal front end of your vision system. Specify high resolution (up to 470,000 pixels) or high sensitivity (up to 600 mV). Choose chips sets, 270,000-pixel color modules, or complete cameras with video output options (composite or Y/C), as well as exposure systems (mechanical or electronic) that can be configured to your needs.

shift: Sharp's putting its opto on the line.

We give you the best data display under any condition: In TFT, you get the contrast, color saturation, fast response and high resolution that has made Sharp far and away the world leader in active matrix displays. In electroluminescent displays, Sharp's unique dual scan drive and tape automated bonding process create a brighter, thinner, more energy efficient display that's ideal for the grit and heat of the factory floor.



combine signal-processing circuitry nd the light-detecting element n a single chip, to save space, ower costs, and raise perfor-mance and component reliability.

Finally, you can look to harp for quality in quantity. rom the broadest line of super-luminosity LEDs to our unique selection of OPICs, our packaging expertise helps us meet more demanding dimensional and environmental specifications — whether off-the-shelf or custom.

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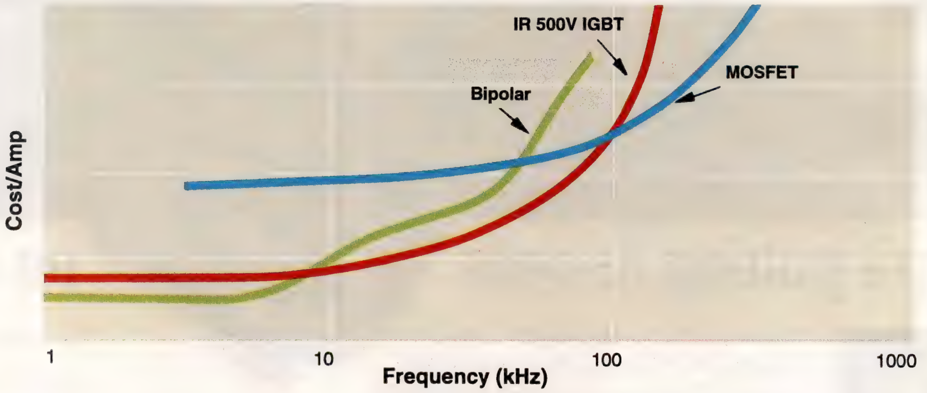

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Our IGBTs also come paired with IR super-soft recovery diodes in *CoPacks* for half-bridge supplies. All give you the lowest conduction losses ever. And fast switching speeds.

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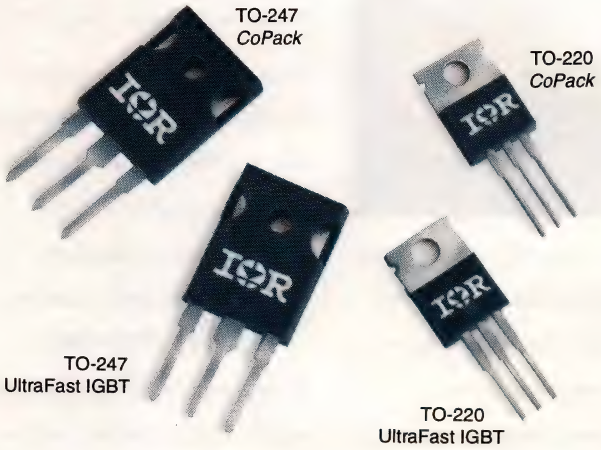

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TECHNOLOGY NEWSLETTER

UPDATED BENCHMARKS SIMPLIFY PLD CHOICE

An improved set of benchmarking test circuits hopes to more accurately reflect the performance and gate capacity of programmable logic devices across various applications. The enhanced suite of tests, developed by the member companies of the Programmable Electronics Performance Corp., Los Gatos, Calif., includes changes to deal with various points that surfaced after the first set of benchmarks was released last year. Some of those issues include the need to assign criticalities homogeneously, and the role that logic-synthesis tools play in removing redundant logic under the step-and-repeat requirements of the PREP benchmarks. Version 1.3, like its predecessor, contains nine commonly used applications that are collectively neutral to all PLD and FPGA architectures and vendors. One change in the new test suite, for example, was the modified design-entry stipulation in Suite #1. Now, every instance of a benchmark case as well as the connections between consecutive benchmark instances must be identical, including the use of criticality. However, any path connected to device pins may have criticality as deemed necessary. In a related activity, PREP has established a new program that allows for independent verification and certification of benchmark data. The Certified Consultant Certification Program thus keeps advanced devices "under wraps." Previously, PREP members had to rely on a "buddy" system under which another PREP member would certify the performance, thus giving a potential competitor an early view of a new chip. Copies of the updated benchmark suite (Version 1.3) and certification guidelines can be obtained from PREP. Contact Kathy Rogers at (408) 356-2169. *DB*

MCM INTERCONNECTS SUBJECT OF PACT

The growing interdependence between interconnect technology and multichip modules (MCMs) lies behind a strategic partnership involving AMP Inc., Harrisburg, Pa., and MicroModule Systems Inc. (MMS), Cupertino, Calif. The companies, which have already partnered on a 486-upgrade MCM with an on-board secondary cache, are considering other possibilities for MCM interconnects, including PCMCIA modules. The relationship is intended to exploit AMP's strengths in board-level and subsystem interconnects with MMS's high-volume MCM technology. Call MMS at (408) 864-7437. *DM*

MODULAR SCHEME EASES NOTEBOOK DESIGN

A general-purpose modular design for small electronic systems, such as notebook and palmtop computers, offers complete system modularization without using screws or flexible cables. The T-Module packaging concept, developed by Free Frame Technologies, San Jose, Calif., enables all components of a system to be assembled or disassembled by hand. According to Winston Hsu, Free Frame's founder, all of the subsystems within portable PCs can be transformed into T-Modules. Consequently, users could quickly and easily upgrade a disk drive, modem, or processor. A clamping and latching scheme builds shock resistance into the concept. Call Hsu at (408) 254-1462. *DM*

JOINT DEVELOPMENT BRINGS INTERACTIVE TV

The ability to view up to seven days of television programming on-screen is now possible. The development came from a joint venture between Zilog Inc., Campbell, Calif., and StarSight Telecast Inc., Fremont, Calif. Zilog's Z89300 TV controller implements the television and VCR technology to support StarSight's proprietary database processor technology. The on-screen interactive programming offers some benefits over traditional guides, such as the ability to scroll through a week's worth of data. In addition, that data can be used to view or record programs using a remote control. The Zilog part will be available in OEM quantities in the second quarter. One-time programmable and engineering sample mask-ROM devices are shipping now. An in-circuit emulator is also available. For more information, call Zilog at (408) 370-8246, or StarSight at (510) 657-9900. *RN*

VIDEOCONFERENCING FOR THE DESKTOP IS COMING

Videoconferencing and telephony on the desktop for less than $7000 is now possible, or at least that's the claim made by Olivetti (UK) Ltd. with its launch of the Personal Communications Computer (PCC). It's basically a personal computer equipped with a British Telecom-designed VC8000 multimedia ISDN adapter. Elias Kanaris, multimedia marketing manager, says he's taking orders now for the machine and promises delivery in February 1994. He explains that prices would depend on the specification of the host computer, but they range from $6500 and up. Olivetti would also sell the VC8000

FILTERS

dc to 3GHz from $\$11^{45}$

lowpass, highpass, bandpass

- less than 1dB insertion loss
- greater than 40dB stopband rejection
- surface-mount
- BNC, Type N, SMA available
- 5-section, 30dB/octave rolloff
- VSWR less than 1.7 (typ)
- rugged hermetically-sealed pin models
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- meets MIL-STD-202 tests
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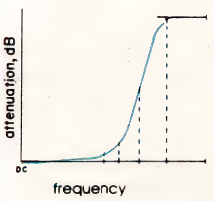
LOW PASS



low pass, Plug-in, dc to 1200MHz

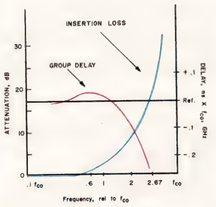
Model No.	Passband MHz loss < 1dB	Stopband, MHz loss > 20dB	Stopband, MHz loss > 40dB
★LP-5	DC-5	8-10	10-200
★LP-10.7	DC-11	19-24	24-200
★LP-21.4	DC-22	32-41	41-200
★LP-30	DC-32	47-61	61-200
★LP-50	DC-48	70-90	90-200
★LP-70	DC-60	90-117	117-300
★P-90	DC-81	121-137	167-400
★LP-100	DC-98	146-189	189-400
★LP-150	DC-140	210-300	300-600
★LP-200	DC-190	290-390	390-800
★LP-250	DC-225	320-400	400-1200
★LP-300	DC-270	410-550	550-1200
★LP-450	DC-400	580-750	750-1800
★LP-550	DC-520	750-920	920-2000
★LP-600	DC-680	840-1120	1120-2000
★LP-750	DC-700	1000-1300	1300-2000
★LP-800	DC-720	1080-1400	1400-2000
★LP-850	DC-760	1100-1400	1400-2000
★LP-1000	DC-900	1340-1750	1750-2000
★LP-1200	DC-1000	1620-2100	2100-2500

Price, (1-9 qty), all models: plug-in $14.95, BNC $32.95, SMA $34.95, Type N $35.95

Surface-mount, dc to 570MHz

SCLF-21.4	DC-22	32-41	41-200
SCLF-30	DC-30	47-61	61-200
SCLF-45	DC-45	70-90	90-200
SCLF-135	DC-135	210-300	300-600
SCLF-190	DC-190	290-390	390-800
SCLF-380	DC-380	580-750	750-1800
SCLF-420	DC-420	750-920	920-2000

Price, (1-9 qty), all models: $11.45

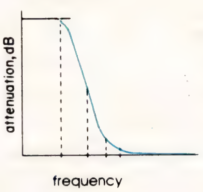


Flat Time Delay, dc to 1870MHz

Model No.	Passband MHz loss < 1.2dB	Stopband MHz loss > 10dB	Stopband MHz loss > 20dB	VSWR Freq. Range, DC thru 0.2fco $\overline{X}$	VSWR Freq. Range, DC thru 0.6fco $\overline{X}$	Group Delay Variations, ns Freq. Range, DC thru fco $\overline{X}$	Group Delay Variations, ns Freq. Range, DC thru 2fco $\overline{X}$	Group Delay Variations, ns Freq. Range, DC thru 2.67fco $\overline{X}$
★BLP-39	DC-23	78-117	117	1.3:1	2.3:1	0.7	4.0	5.0
★BLP-117	DC-65	234-312	312	1.3:1	2.4:1	0.35	1.4	1.9
★BLP-156	DC-94	312-416	416	0.3:1	1.1:1	0.3	1.1	1.5
★BLP-200	DC-120	400-534	534	1.6:1	1.9:1	0.4	1.3	1.6
★BLP-300	DC-180	600-801	801	1.25:1	2.2:1	0.2	0.6	0.8
★BLP-467	DC-280	934-1246	1246	1.25:1	2.2:1	0.15	0.4	0.55
▲BLP-933	DC-560	1866-2490	2490	1.3:1	2.2:1	0.09	0.2	0.28
▲BLP-1870	DC-850	3740-6000	5000	1.45:1	2.9:1	0.05	0.1	0.15

Price, (1-9 qty), all models: plug-in $19.95, BNC $36.95, SMA $38.95, Type N $39.95
NOTE: ▲: -933 and -1870 only with connectors, at additional $2 above other connector models.

HIGH PASS

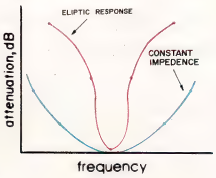


high pass, Plug-in, 27.5 to 2200MHz

Model No.	Stopband MHz loss < 40dB	Stopband MHz loss < 20dB	Passband, MHz loss < 1dB	VSWR Passband Typ.
★HP-25	DC-13	13-19	27.5-200	1.8:1
★HP-50	DC-20	20-26	41-200	1.5:1
★HP-100	DC-40	40-55	90-400	1.8:1
★HP-150	DC-70	70-95	133-600	1.8:1
★HP-175	DC-70	70-105	160-800	1.5:1
★HP-200	DC-90	90-116	185-800	1.6:1
★HP-250	DC-100	100-150	225-1200	1.3:1
★HP-300	DC-145	145-170	290-1200	1.7:1
★HP-400	DC-210	210-290	395-1600	1.7:1
★HP-500	DC-280	280-365	500-1600	1.8:1
★HP-600	DC-350	350-440	600-1600	2.0:1
★HP-700	DC-400	400-520	700-1800	1.6:1
★HP-800	DC-445	445-570	780-2000	2.1:1
★HP-900	DC-520	520-660	910-2100	1.8:1
★HP-1000	DC-550	550-720	1000-2200	1.9:1

Price, (1-9 qty), all models: plug-in $14.95, BNC $36.95, SMA $38.95, Type N $39.95

BANDPASS



bandpass, Elliptic Response, 10.7 to 70MHz

Model No.	Center Freq. (MHz)	Passband I.L. 1.5 dB Max. (MHz)	3 dB Bandwidth Typ. (MHz)	Stopbands I.L. > 20dB at MHz	Stopbands I.L. > 35dB at MHz
★BP-10.7	10.7	9.6-11.5	8.9-12.7	7.5 & 15	0.6 & 50-1000
★BP-21.4	21.4	19.2-23.6	17.9-25.3	15.5 & 29	3.0 & 80-1000
★BP-30	30.0	27.0-33.0	25-35	22 & 40	3.2 & 99-1000
★BP-60	60.0	55.0-67.0	49.5-70.5	44 & 79	4.6 & 190-1000
★BP-70	70.0	63.0-77.0	68.0-82.0	51 & 94	6.0 & 193-1000

Price, (1-9 qty), all models: plug-in $18.95,
BNC $40.95, SMA $42.95, Type N $43.95

Constant Impedance, 21.4 to 70MHz

Model No.	Center Freq. MHz	Passband MHz loss < 1dB	Stopband loss > 20dB at MHz	VSWR 1.3:1 Total Band MHz
★IF-21.4	21.4	18-25	1.3 & 150	DC-220
★IF-30	30	25-35	1.9 & 210	DC-330
★IF-40	42	35-49	2.6 & 300	DC-400
★IF-50	50	41-58	3.1 & 350	DC-440
★IF-60	60	50-70	3.8 & 400	DC-500
★IF-70	70	58-82	4.4 & 490	DC-550

Price, (1-9 qty), all models: plug-in $14.95,
BNC $36.95, SMA $38.95, Type N $39.95

NOTE: ★**Add Prefix P, B, N, or S for Pin, BNC, N, or SMA connector requirement.**

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F132 1-2 REVC

ISDN video adapter card as a separate accessory for a price of $4500. Initially, the PCC will be made available only in the U.K. However, through its newly formed Telecommunications and Multimedia Division, Olivetti will market the system later on throughout Europe. *PF*

DIGITAL TVS TO ADOPT MPEG-2 STANDARD

Digital TV receivers based on the MPEG-2 video and audio compression standard will be ready for market in the U.K. by the third quarter of 1994. Or so says Alan Watson, manager for advanced products for TV engineering and research company National Transcommunications Ltd. (NTL), Winchester, England. Some 85 European broadcasting network operators, TV equipment manufacturers, and governments already signed a memorandum of understanding last fall agreeing that all future European digital TV standards will be based on the MPEG-2 video and audio compression standards. As a result, satellite operators are planning to start direct-to-home digital TV services in 1995. The MPEG-2 standard allows compression of up to 10 TV channels into the bandwidth currently occupied by just one analog channel. NTL allied with a volume manufacturer of satellite and terrestrial broadcast receivers, Pace Micro Technology Ltd., Bradford, England, to produce a range of digital satellite, cable, and terrestrial broadcast receivers and decoders. Both companies have been appointed to the steering board of the Digital Video Broadcasting project aimed at defining European standards for digital TV. For more information, contact NTL at +44 (0)962 822562, or Pace Micro Technology at +44 (0)274 532000. *PF*

MULTIMEDIA ISDN CARD READIED FOR PRODUCTION

An ISDN adapter card that brings full multimedia services to a personal computer, including video telephone and interactive desktop data conferencing, has been awarded full certification by the British Approvals Board for Telecommunications (BABT). Designed by British Telecommunications plc (BT) in collaboration with Motorola Semiconductor Products, IBM UK Ltd., and Ing. Olivetti Spa., the VC8000 card will enter full production on a dedicated manufacturing line at the Automotive and Industrial Electronics Group of Motorola Ltd. in the U.K. The next phase in the card's two-year development cycle is scheduled to begin in January 1994, when a first production batch of 250 units will be supplied to 40 companies for the final stages of operational testing in the field. Each of the firms will pay $4500 for their cards. This "beta" trial phase, scheduled for completion by the spring of 1994, is intended to identify any possible final changes to software or hardware. Full commercialization under the IBM and Olivetti brand names is slated for June 1995. *PF*

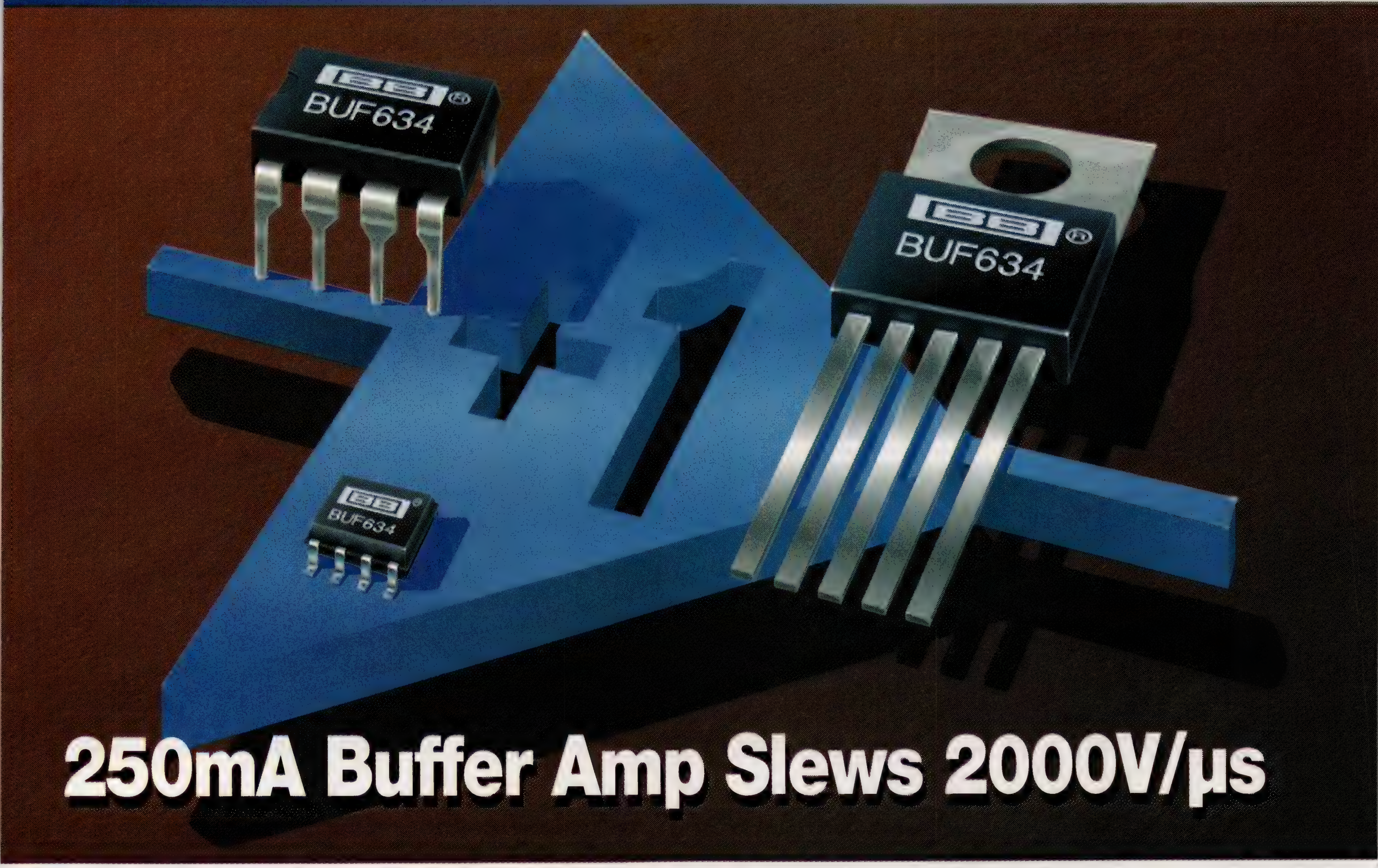
PROGRAM AIMS TO IMPROVE BATTERIES

A partnership between Sandia National Laboratories, Albuquerque, N.M., and four U.S. companies is shooting for better rechargeable batteries to power communications equipment and other portable systems. A cooperative R&D agreement between Sandia and AT&T Bell Labs, Murray Hill, N.J.; Eveready Battery Co., St. Louis, Mo.; Rayovac Corp., Madison, Wis.; and Wilson Greatbatch Ltd., Clarence, N.Y.; will forge toward identification and characterization of a carbon material to be used as an anode for rechargeable lithium-ion batteries. By pinpointing such a material, it's hoped that the lithium-ion cells now being introduced by Japanese companies to power cellular telephones and camcorders can be improved. These batteries already offer the high voltages and energy levels of metallic lithium systems while extending safety advantages and improved cycle life. The sought-after carbon material for the anode would efficiently and reversibly insert lithium ions into the carbon lattice. Using the engineered carbon, the four companies plan to design batteries with higher energy and longer cycle lives than existing rechargeables. This would enable U.S. manufacturers to better compete in the portable-system market. For more information, contact Sandia's Sam Levy at (505) 844-8029. *DM*

INPUT SLOPE MODELING SPEEDS IC DESIGN

A new input-slope modeling (ISM) technique used in library-development tools will speed the characterization of deep submicron ASICs. Compass Design Automation Inc., San Jose, Calif. has come up with a highly accurate ISM technology that requires fewer circuit simulations for CMOS cell characterization than other ISM approaches. Typical ISM methods need an average of 20 to 30 Spice simulations per input pin. However, the Compass ISM method needs only four Spice simulations per pin. This results in faster overall circuit simulation runs and more efficient data collection for the cell-characterization process. The Compass modeling maintains accuracy to within 5% of Spice for almost all temperature, voltage, and process-technology conditions. In addition, to ensure that simulation values are accurate for varying conditions, engineers can apply scaling factors for each term in a delay equation rather than use just one factor for the entire equation. Call Compass Design Automation at (408) 433-4880. *LM*

NEW



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BUF634 can be used inside the feedback loop of op amps to increase output current, eliminate thermal feedback, and improve capacitive load drive. Its bandwidth can be pin-programmed for 30MHz with 1.5mA quiescent current or boosted to 180MHz with 15mA quiescent current. BUF634 is the simple solution for all your buffer needs.

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BUF634's monolithic design is very rugged—its internal current limit and thermal shutdown protect it from extreme abuse. BUF634 withstands load faults and short-circuits with ease. It's virtually indestructible—you can design-in this device with confidence.

BUF634 Key Specifications

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• Pin-selected bandwidth	30MHz to 180MHz
• Quiescent current	1.5mA (30MHz BW)
• Supply range	±2.25V to ±18V
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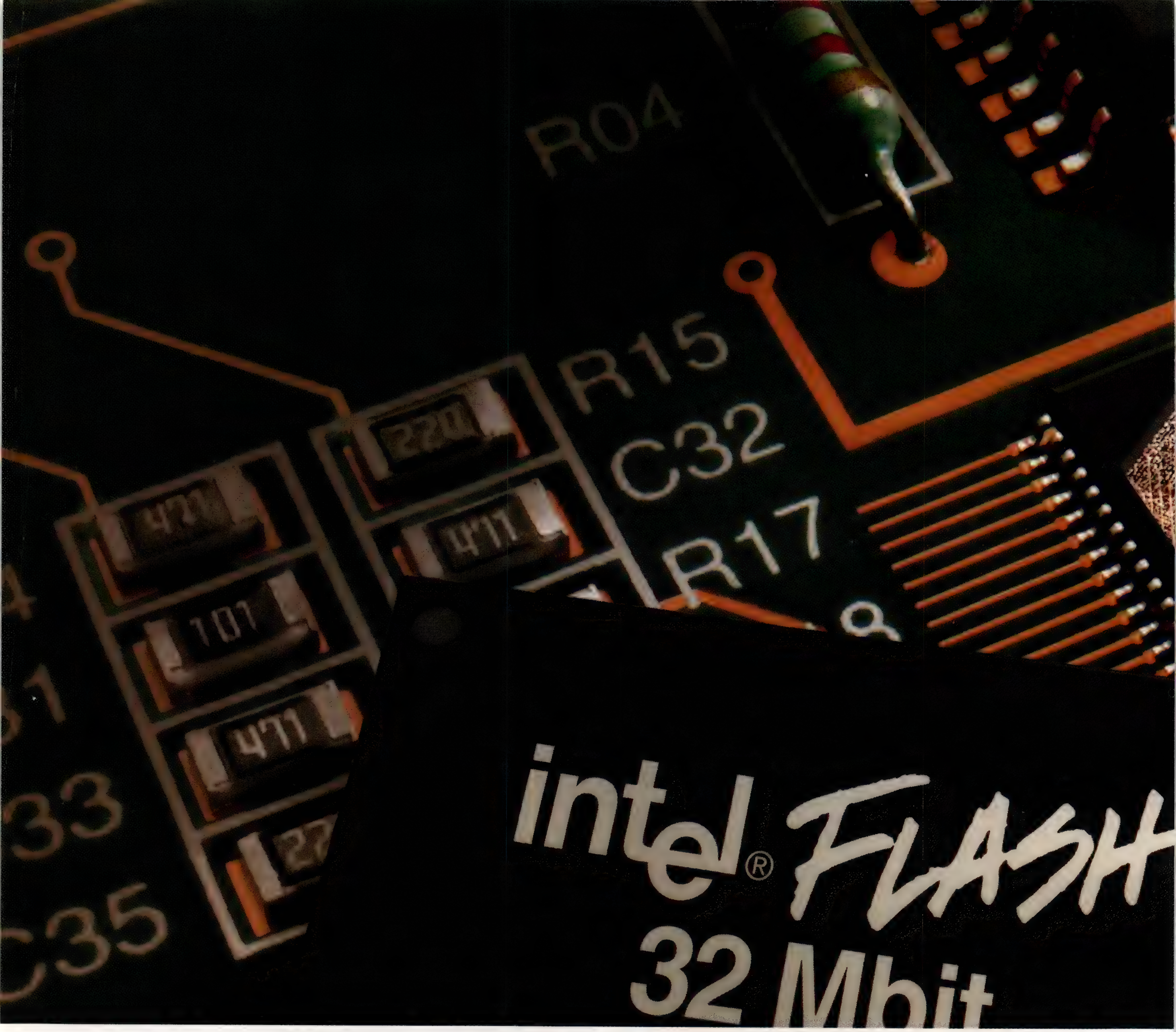

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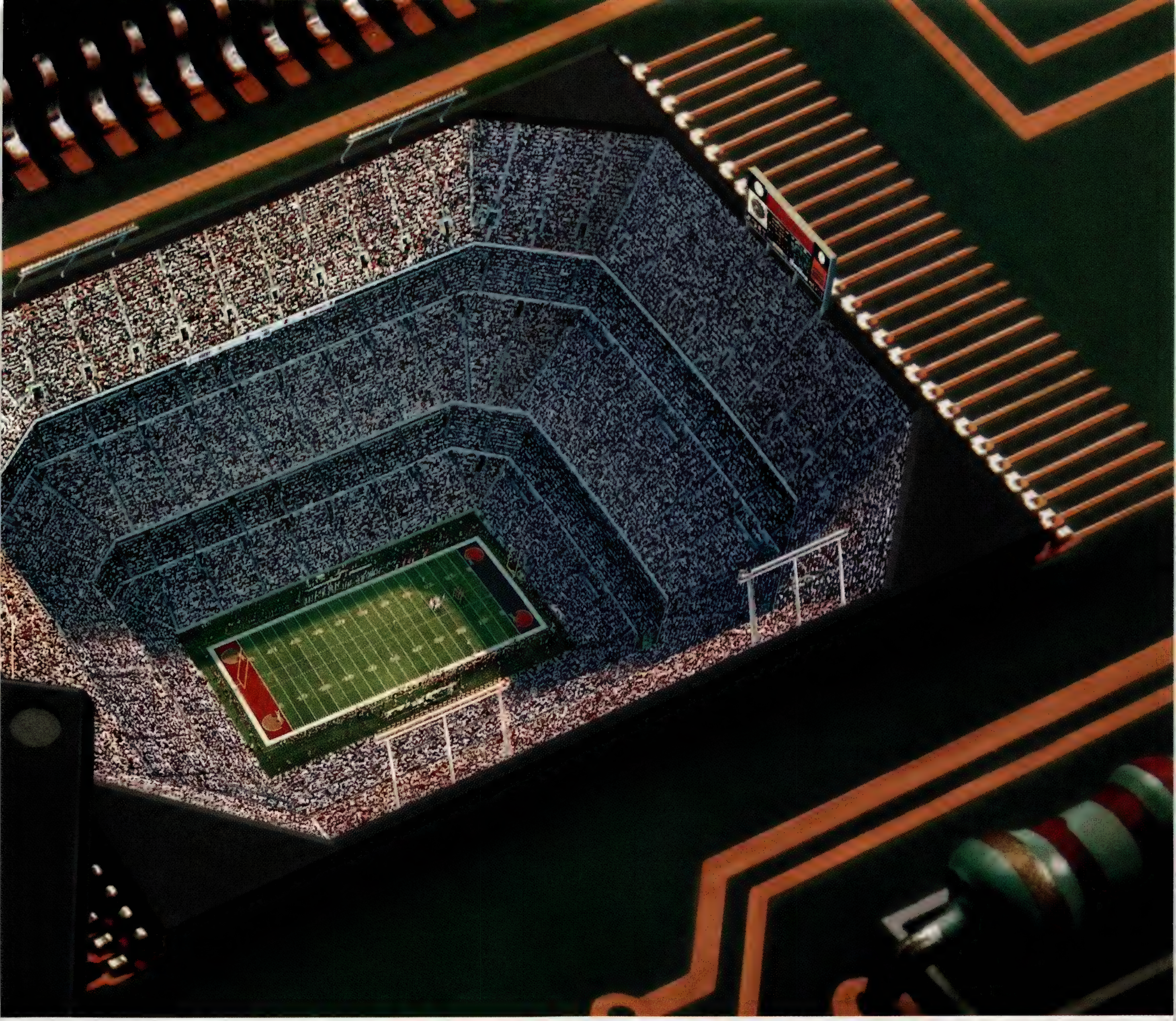

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current consumption down to a 1 to 2mA static mode, while sleep mode further drops it to just 1 to 2µA.

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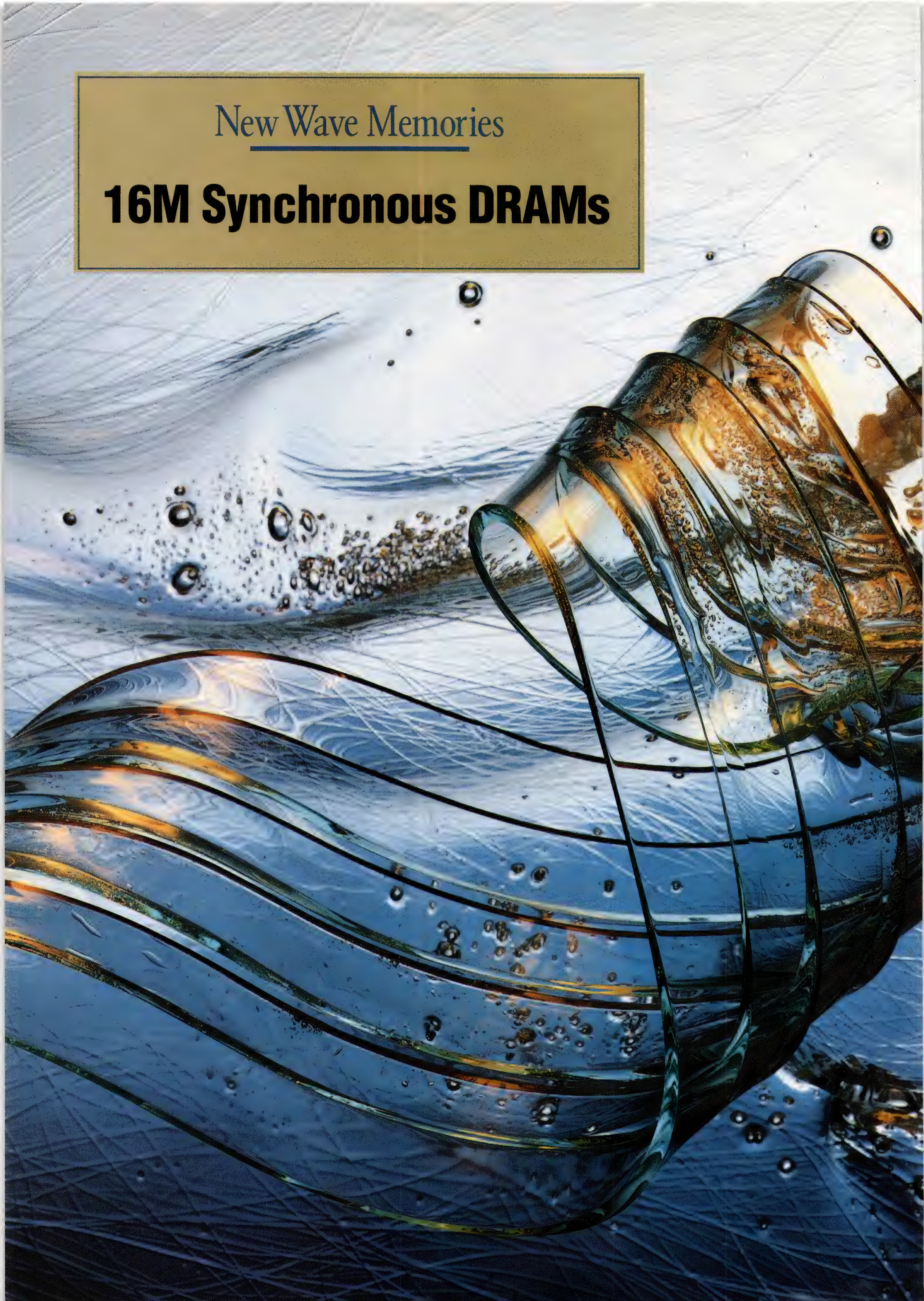
New Wave Memories

16M Synchronous DRAMs



Forget about cost/performance trade-offs. Our new 16M Synchronous DRAMs give you big benefits in both areas. Operating at 100MHz clock, they eliminate CPU wait states. So workstation designers save by eliminating costly cache SRAMs. And PC designers gain a quantum leap in system speed.

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READER SERVICE 99

NEC

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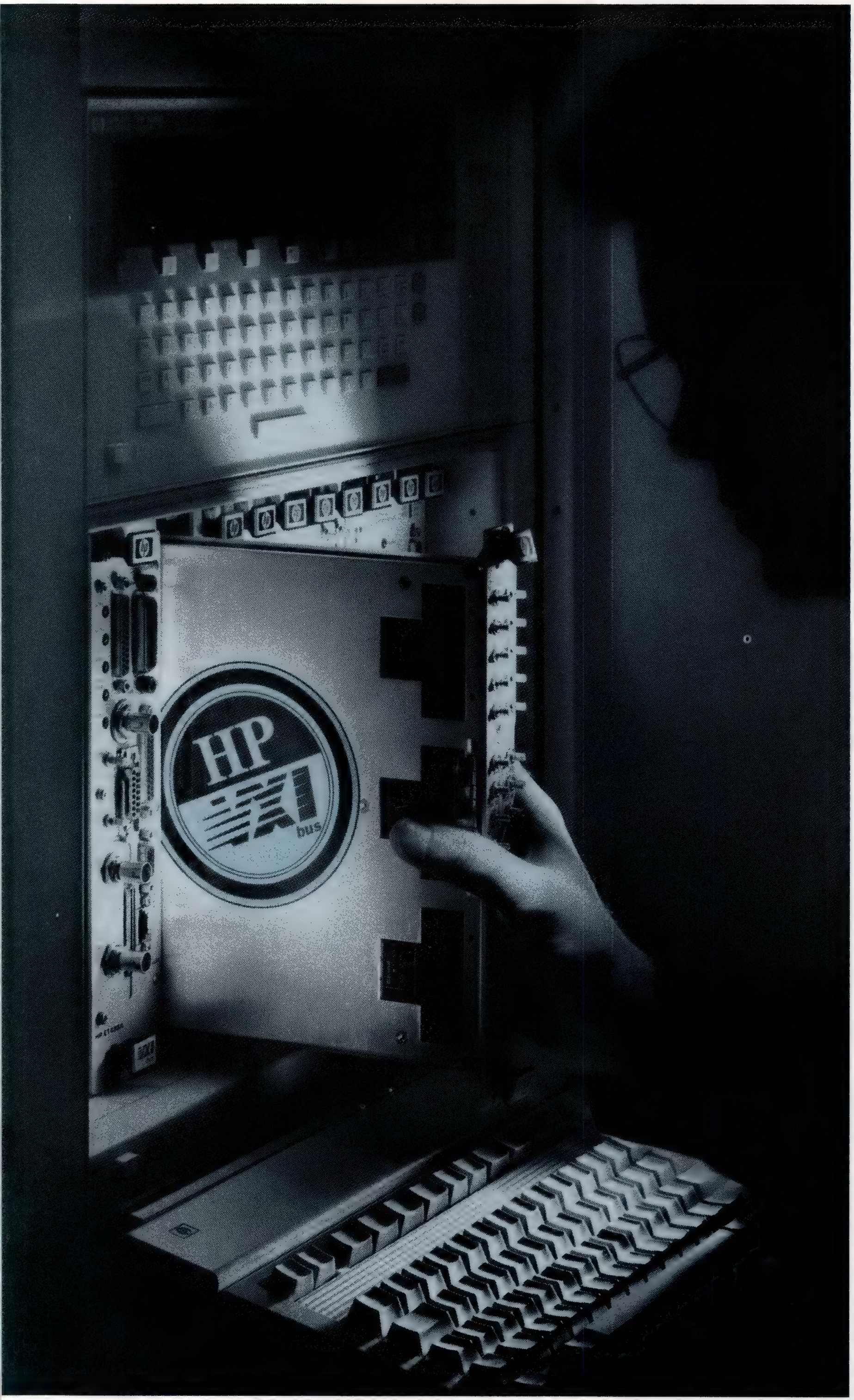

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READER SERVICE 131

OPERATING SYSTEM MIMICS REAL-WORLD FUNCTIONS TO SIMPLIFY OPERATION

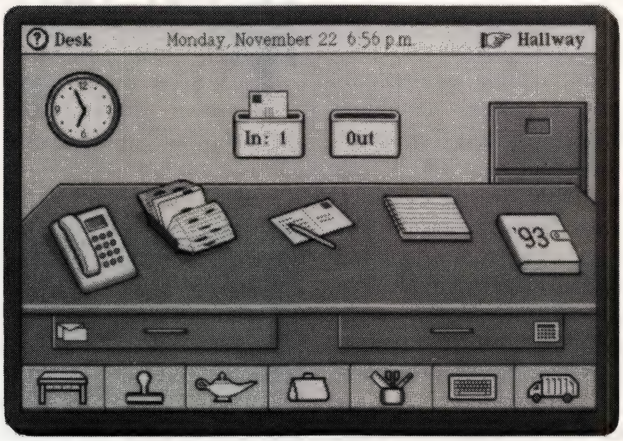
Although graphical user interfaces aren't new, available GUIs for personal digital assistants are now transforming PDAs into a real substitute for the desktop and the telephone. Using graphical desktop metaphors—telephones, in and out baskets, file cabinets, drawers, and many other office items—lets users interpret the images quickly into real-world functions. The ease of understanding creates a simplicity of use rarely seen in computing appliances.

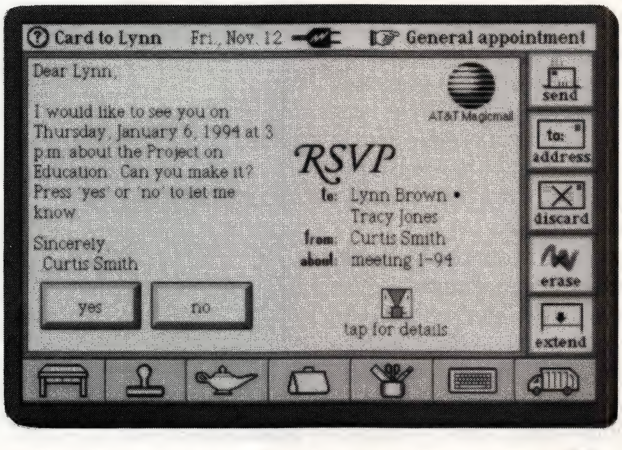
To that end, developers at General Magic Inc., Mountain View, Calif., came up with the most real-world-like GUI/operating system to date for PDAs and consumer digital appliances, called Magic Cap. In addition to the operating system, which would be embedded in the appliance, designers at General Magic worked in concert with AT&T to develop an intelligent communications schema and a scripting language, dubbed Telescript. Telescript also can be employed independently from Magic Cap as a system extension onto any personal communicator or computer platform.

To make possible such a development, General Magic worked with a number of partner companies—Apple Computer, AT&T, Motorola, Philips, and Sony. These partners provided the multiplicity of resources needed for an integrated, communications-centric graphical operating system, and defined the base hardware platform on which it runs.

The GUI/OS is tightly integrated with the communications capability so that users don't have to think twice about how to send messages or take action on incoming requests. Part of the software, for example, monitors incoming messages and will automatically update the address directory with new contact information. Or it will update existing contacts if the incoming message/request has a new address, telephone number, etc. Furthermore, if the software is running on both a PDA and a host desktop system, all addresses, appointments, and other items will be updated and reconciled when the two are connected.

The Magic Cap software is founded on a multithreaded object-oriented operating system. It's a collection of frameworks, with each application, including the built-in applications, tightly coupled to the frameworks. Third parties can add extra functionality, modify existing capabilities, and create new communicating packages. With the multithreading, asynchronous tasks (both background and foreground) are managed, including power management. The smart power management incorporated into the system gives every power-consuming hardware subsection a software module that tells the host processor how much power it needs.





Dear Lynn,

I would like to see you on Thursday, January 6, 1994 at 3 p.m. about the Project on Education. Can you make it? Press 'yes' or 'no' to let me know.

Sincerely,
Curtis Smith

to: Lynn Brown •
Tracy Jones
from: Curtis Smith
about: meeting 1-94

About 3 Mbytes of ROM are needed to hold the Magic Cap software (program and image storage) and about 300 kbytes of RAM are used for transient execution space. Although initially developed to run on the recently introduced M68349 "Dragon" processor developed by Motorola Inc., Austin, Texas, the software will also be available on the Apple Macintosh and on IBM-compatible PCs running Windows. The Dragon chip is based on a 32-bit 68030 CPU core and includes many on-chip peripherals, such as a DMA controller, serial channels, timers, and memory control. A fully-static processor, the Dragon chip can operate at 3.3 V, consuming just 300 mW at 16 MHz and 1 mW when idling.

The minimum hardware configuration for Magic Cap, as defined by General Magic in its minimum functionality specification, will initially consist of a 68349-based system with a 2400-baud fax modem, 3 Mbytes of ROM, 1 Mbyte of RAM, a built-in speaker and microphone, a PCMCIA-compatible card interface, and a 480-by-320-pixel (minimum) touch screen. For communications with a host computer or peripherals, the base system will also include a low-speed infrared serial interface (HP-compatible), and a proprietary but open-specification high-speed serial expansion bus (Magic Bus) that runs at rates from several hundred kbits/s to over 14 Mbits/s.

To appreciate the uniqueness of Magic Cap, one really has to sit down and use it. The desktop metaphor as well as the images and sounds not only make it easy to use, but also make it fun—a rarity in today's business world. Although most operations are centered around the desktop with its telephone, address file, in and out baskets, filing cabinet, etc., that metaphor is only one level of the OS *(see the figure, top)*.

The desktop represents a "room." By tapping on the touch screen, users can leave the room and walk down an animated and custom-decorated "hallway" that lets them reach other rooms. Each room represents an application, whether it be a library, a database, a spreadsheet, or even a second desktop metaphor setup, perhaps, as an accountant's lair. The room/hallway metaphor can be expanded even one level higher, in which the user can go from "building" to "building" while "walking" downtown. Buildings represent entire domains, such as shopping services, communication services, and other services that the PDA can link into.

The object-oriented foundation allows everything from the icons to the entire application to carry their own characteristics, making them easily "attachable." This allows objects to be linked to an application. One such example of that is the collection of icons or "stamps" built into the GUI/OS. These stamps can be copied onto any screen to annotate documents or screens with static or animated labels, such as "urgent," smiling or sad faces, stones rolling downhill, animals running or hopping, push-button response buttons, and stored sounds—personal messages or prerecorded sound effects.

The Telescript communications scripting scheme is unparalleled in the industry. Other communication packages only send out passive information—a fax, a linkup/data exchange with a host system, etc. Telescript, on the other hand, can also send out intelligent packets called agents. Each agent encapsulates a message, a request for information, or even an information filter. The user would create an agent by producing a script of what must be done—for example, "access image database xxx and find all images that include telephones."

All user instructions (the script) get encapsulated into a message (an agent) that's sent to the communications network "cloud." In the cloud, the agent gets routed to the desired information, takes action (performs database searches, sets up flight itineraries, transfers messages), and passes the result of the action back to the original sender. Previous interfaces typically would just interrogate a database, transfer a file, or handle a simple business transaction. However, no preprocessing took place in the network.

One simple example of agent usage combines Magic Cap and Telescript. Under Magic Cap, a user may want to create an electronic message that's sent to one or more associates to set up a meeting. To do that, a postcard metaphor can be pulled up on the screen, with the recipient's name and address filled in from an address book and a message entered with the date, location, and time of the meeting *(see the figure, bottom)*. In addition to the message, special reply buttons (yes and no, for example) could be attached so the recipient can respond to the message immediately.

When the message is received by an addressee, the "postcard" metaphor bears a postmark, indicating the date and time the message was received. Attached icons like the "urgent" stamp actually do more than just annotate the card—they can be miniagents. In the case of the urgent stamp, this miniagent moves the postcard ahead of non-urgent messages in the "in basket."

Similarly, if the recipient pushes the "yes" or "no" button images, those miniagents cause the recipient's system to send a message back to the originator, giving a yes or no response to the originator. If it's a "yes", the intelligence included in the Magic Cap software puts the meeting information in the recipient's calendar and also adds the respondent's name to the meeting calendar in the originator's system.

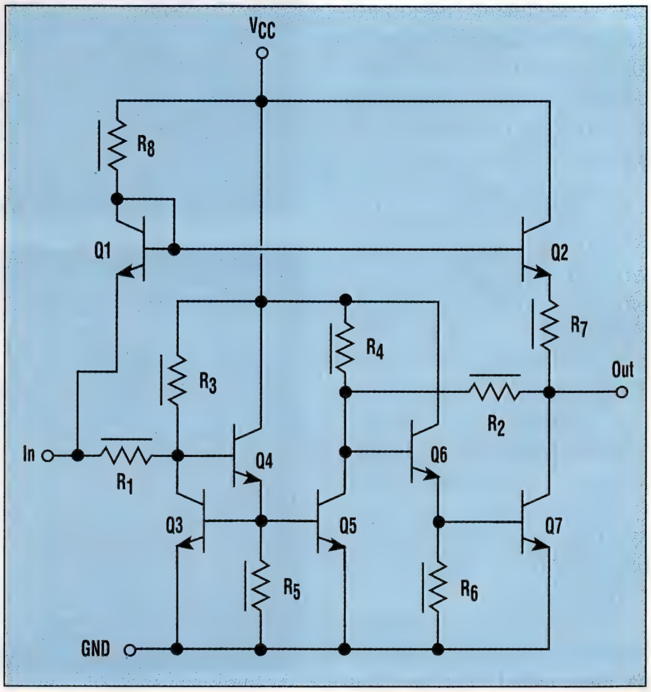
Both Magic Cap and Telescript, unveiled last month at the MacWorld Conference and Exhibition in San Francisco, Calif., can be licensed from General Magic. Currently over 20 developers are crafting both portable and desktop platforms, application packages, peripherals, and even support chips. Mitsubishi Electronics America Inc., Sunnyvale, Calif., for instance, developed a microcontroller with the Magic Bus interface embedded on the chip. Such a chip will considerably simplify the design of peripherals that would attach to the PDA, or a base station that the PDA could plug into.

For more information, contact General Magic's Joanna Hoffman at (415) 261-3860.

DAVE BURSKY

ANALOG SCHEME IMPROVES DIGITAL TRANSCEIVER

Typically, transceivers for digital buses are implemented with digital logic that buffers the input and delivers a strong signal to drive highly capacitive loads. Traditional circuit schemes, however, add 3 to 5 ns of propagation delay to the input signal. An improved scheme, which banks on



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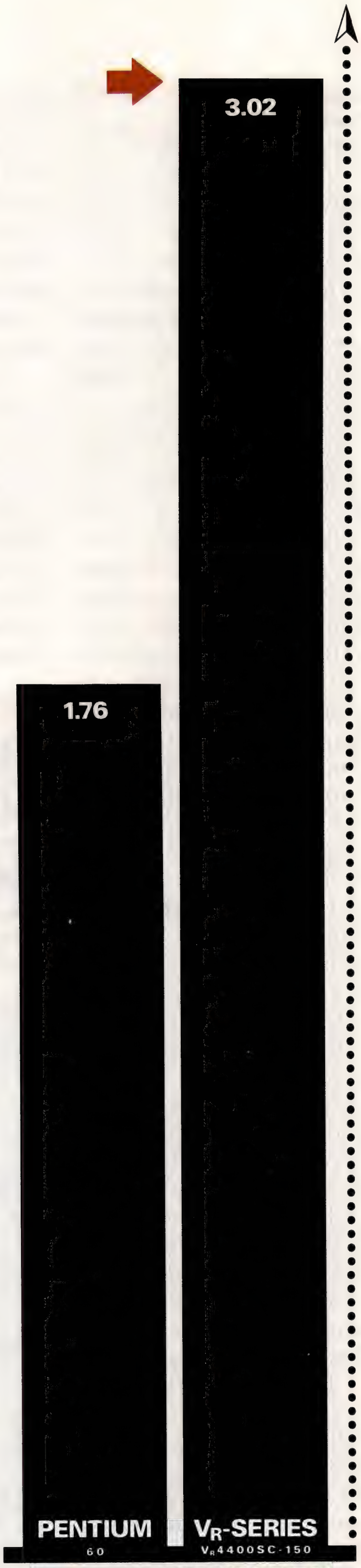

BYTE BENCHMARK
PERFORMANCE RELATIVE TO 486-66

NEC

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READER SERVICE 100

analog-feedback circuit techniques, keeps the input-to-output delay to just 1.5 ns for an octal transceiver. The scheme, developed by Micro Linear Corp., San Jose, Calif., avoids using cascaded inverter stages that progressively employ larger transistors to buffer the input signal. Rather, designers at the company implemented a biCMOS octal transceiver using npn transistors for the amplifier/buffer cell and MOS elements for support logic. The buffer includes npn transistors to achieve the shortest delays, while MOS devices are used in the surrounding circuits to place the dormant buffers into a three-state mode. Such a combination yields typical rise and fall times of 1.2 ns with a 50-pF load at clock frequencies of 50 MHz and higher.

In the buffer, the assertion path starts with an emitter follower comprising a level-shift transistor (Q1), an output transistor (Q2), and a bias resistor (R_8) *(see the figure)*. That circuitry sources current to the output through the 75-Ω resistor (R_7), which is bypassed by another npn transistor *(not shown)* during fast input transients. The negation path is a current-differencing operational amplifier connected in a follower configuration.

The amplifier consists of transistors Q3-Q7; bias resistors R_3-R_6; and two feedback resistors, R_1 and R_2. In the current-differencing amplifier, the currents in transistors Q3 and Q5 are always identical, and the voltages at the bases of Q4 and Q6 are roughly the same.

If the output is higher than the input, an error current will flow through R_2. This error current will flow into the base of Q6 and be multiplied by β^2 to the collector of Q7, which closes the loop. The greater the discrepancy between the output and the input, the larger the feedback current and the harder Q7 sinks current from the load capacitance.

Several of the resistors were implemented as resistive transmission gates to ensure that disabled buffers don't load the lines to which they're connected. Furthermore, in series with R_8 is a p-channel transistor *(not shown)* that's usually turned on, but shuts off when the buffer is disabled to help minimize current drain. Quiescent current for the buffer is about 7 mA, but drops to less than 10 µA when the buffer becomes disabled.

R_7 also acts as a termination resistance. Because it's connected in series with the output, it can suppress noise caused by transmission-line effects such as reflections from mismatched impedances. This keeps the ground-bounce noise to less than 300 mV. In contrast, system designers using CMOS transceivers would typically have to add external resistors in series with each transceiver output to suppress this noise. In addition, an internal diode clamp improves the circuit settling time.

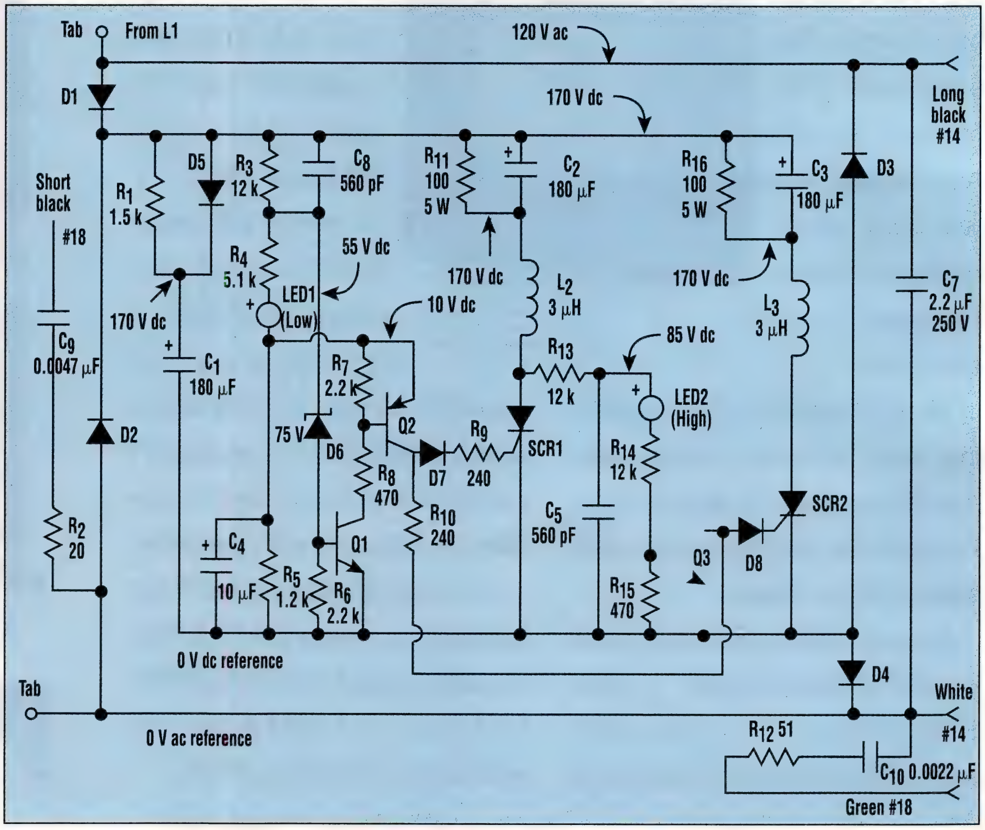
To prove out this concept, designers at Micro Linear incorporated this buffer in an octal transceiver, the ML6580. It's the first transceiver to use all analog circuitry to implement the digital buffering function. The circuit operates with less than half the added delay of other transceivers, giving system designers more timing margin to use when computing system timing. Contact Ram Gopalan, (408) 433-5200.

DAVE BURSKY

SERIES-MODE SUPPRESSION SUBDUES SURGES SAFELY

Knowledgeable and informed computer users certainly are aware that their equipment should bear some kind of protection against the potentially lethal effects of power-line surges. Many, in fact, have installed metal-oxide-varistor (MOV) transient suppressors either in the equipment itself or in the power strips the equipment is plugged into.

The typical MOV-based protection scheme shunts surges from the hot power line into the neutral and ground wires in a process



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To make a long story short, two-thirds into the newspaper phase, Celebrity's ships were just about full to the end of the season. With so little left to sell, we all agreed to hold the radio and TV and save the remainder of the budget.

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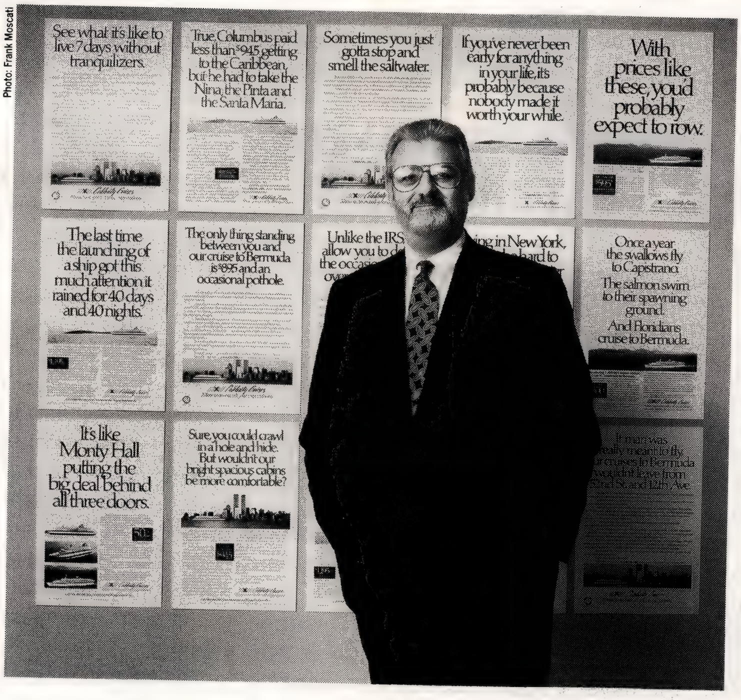
See what it's like to live 7 days without tranquilizers.
True, Columbus paid less than $945 getting to the Caribbean, but he had to take the Nina, the Pinta and the Santa Maria.
Sometimes you just gotta stop and smell the saltwater.
If you've never been early for anything in your life, it's probably because nobody made it worth your while.
With prices like these, you'd probably expect to row.
The last time the launching of a ship got this much attention it rained for 40 days and 40 nights.
The only thing standing between you and our cruise to Bermuda is $895 and an occasional pothole.
Once a year the swallows fly to Capistrano. The salmon swim to their spawning ground. And Floridians cruise to Bermuda.
It's like Monty Hall putting the big deal behind all three doors.
Sure, you could crawl in a hole and hide. But wouldn't our bright spacious cabins be more comfortable?

Photo: Frank Moscati

Al Wallack, Sr. VP Marketing, Celebrity Cruises, after returning from having his hearing checked.

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that's often described as "all three modes of protection." According to Rudy Harford, chief engineer at Zero Surge Inc., Frenchtown, N.J., such a scheme is failure-prone and potentially dangerous both to the computer user and the precious data it processes. Zero Surge came up with a series-mode surge-suppression methodology that deals with both internal and external disturbances in a safe, effective manner.

Although they can be effective in stopping surges, MOVs have weaknesses that, over time, can make them more of a hindrance than a help. For one, they have a limited lifetime. Each time a surge that surpasses a modest threshold reaches an MOV, it degrades somewhat and eventually is rendered ineffective. The typical failure mode for an MOV is overheating—they've been known to explode and/or burn.

Another problem with MOV-based surge suppression lies in the way they are applied. Typically, MOVs are connected across the hot and neutral wires at some distance from the ground node. As noted earlier, their impedance can become very low over time. When subjected to an external disturbance (one that enters by way of a building's electrical-service entrance) that causes them to conduct, the disturbance voltage, or what remains of it when you subtract the MOV's clamping voltage, is divided between the hot and neutral lines in proportion to the two lines' respective impedances.

Because these impedances are typically equal, about half the disturbance voltage will appear on the neutral (common) wire with respect to the ground wire. This common-mode voltage can exceed 2000 V with respect to ground, stressing the equipment's common-mode capability. It can then capacitively couple across the isolating circuits and into the equipment itself. In effect, then, the MOV is transferring the disturbances to ground. The results can be catastrophic, especially when the equipment relies on the power-line ground circuit for a reference voltage.

In the Zero Surge series-mode suppression scheme, the surge that enters the circuit first sees a current-limiting choke in series with the line *(see the figure)*. That choke is followed by a voltage-limiting bridge, which presents a far lower impedance to the surge than does the equipment it's protecting. Within this bridge, the surge energy is stored by three large electrolytic capacitors. One of the three capacitors is charged to track the sine-wave peak at all times. When a surge does hit, the excess energy flows into the other two capacitors. They slowly release their energy back into the neutral line through current-limiting resistors.

The series-mode methodology is equally effective in deadening internally generated transients, which can have extremely fast rise times of up to 40 kV/µs. Such transients evolve from voltages of equal and opposite polarities that are developed on the hot and neutral wires with respect to ground when current in those lines is interrupted by switching. Simple shunt suppression of these surges is impractical, because an MOV is too slow to react.

Addressing that problem, Zero Surge's methodology uses snubbers consisting of a resistor in series with a capacitor. Snubbers are frequency selective, they work instantaneously, and have no threshold to be exceeded before they act. In fact, they can cut internal disturbances below the normal conduction level of conventional shunt suppressors.

For more information, contact Zero Surge at (908) 996-7700.

DAVID MALINIAK

SCSI CONNECTOR STANDARD SIMPLIFIES CONFIGURATION

A proposed standard for SCSI connectors, called the Single Connector standard, aims to simplify the installation of SCSI peripherals. It would encompass all of the critical elements needed for peripherals to migrate to fast and wide SCSI implementations. The standard also eliminates any problems associated with the tangle of many wires and cables. The connector was proposed by Sun Microsystems, Mountain View, Calif.; Seagate Technology, Scotts Valley, Calif.; and other disk-drive manufacturers.

Installing the hardware portion of a SCSI device, such as a hard-disk drive, can be a complex task. For example, the user must physically mount the drive within the cabinet. Power cables must be attached, and a series of jumpers must be set to ensure proper SCSI operation. For visual indication of drive operation, another cable attachment is needed for the activity LED. For applications that require several drives (e.g. disk arrays), yet another connection must be made for an external clock signal to obtain synchronized spindle rotations.

Under the standard, a single connector holds the power and interface connectors, the SCSI ID jumpers, the LED signal, and other functions to create a single point of contact for all necessary connections. Within the connector is the full complement of interface signals needed for the 8-bit bandwidth of the standard SCSI interface. Additional lines are available for 16-bit support. The standard also includes a provision to set a device's SCSI ID through software using four designated signal lines.

Other connector features are delayed and remote spindle start. A delayed start is necessary for systems that need a little extra time to initialize the host before the drives come on-line. The remote startup lets the host control at what instance the drive's spindle motor is initiated. This feature is typically required by drives that are assigned a specific function, such as backup, because they aren't always on-line. As a result, the drive is only turned on when it's needed.

The specification calls for 5- and 12-V power, with a dedicated ground for each. Specifically, there are four each of the +12- and +5-V power lines, as well as four each of the +12- and +5-V ground lines. The power and ground pins are strategically positioned on the connector to mitigate the effects of EMI, preventing the corruption of data that's passed over the SCSI bus.

For more information, contact Seagate Technology at (408) 438-8111.

RICHARD NASS

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System Implications of ATM
Dr. Daniel Abensour, ATM Systems Manager,
IBM Corp.

Network Component Directions
Charles Carinalli, Senior V.P and Chief Technical
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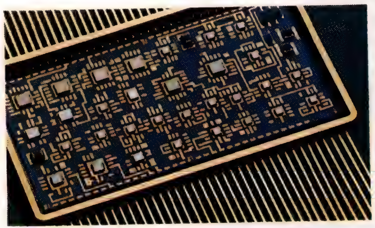

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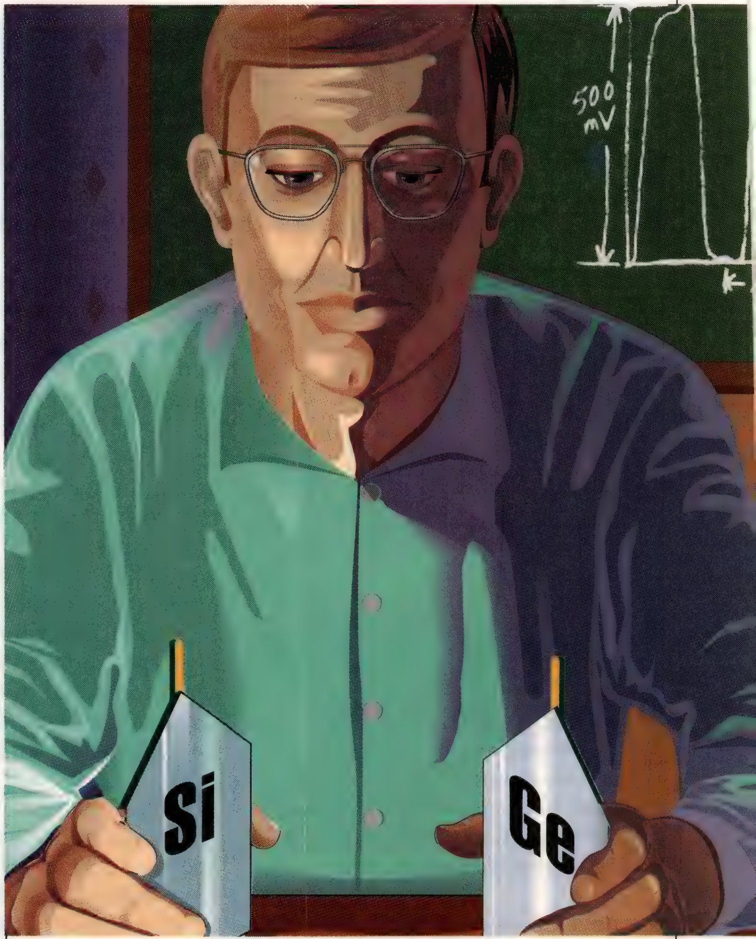
SiGe Heterojunction Bipolar Transistors Form A Current-Output DAC That Operates On Just One Watt Of Power.

12-BIT DAC RUNS AT 1 GHZ, PUTS 20 MA INTO 50 Ω

FRANK GOODENOUGH

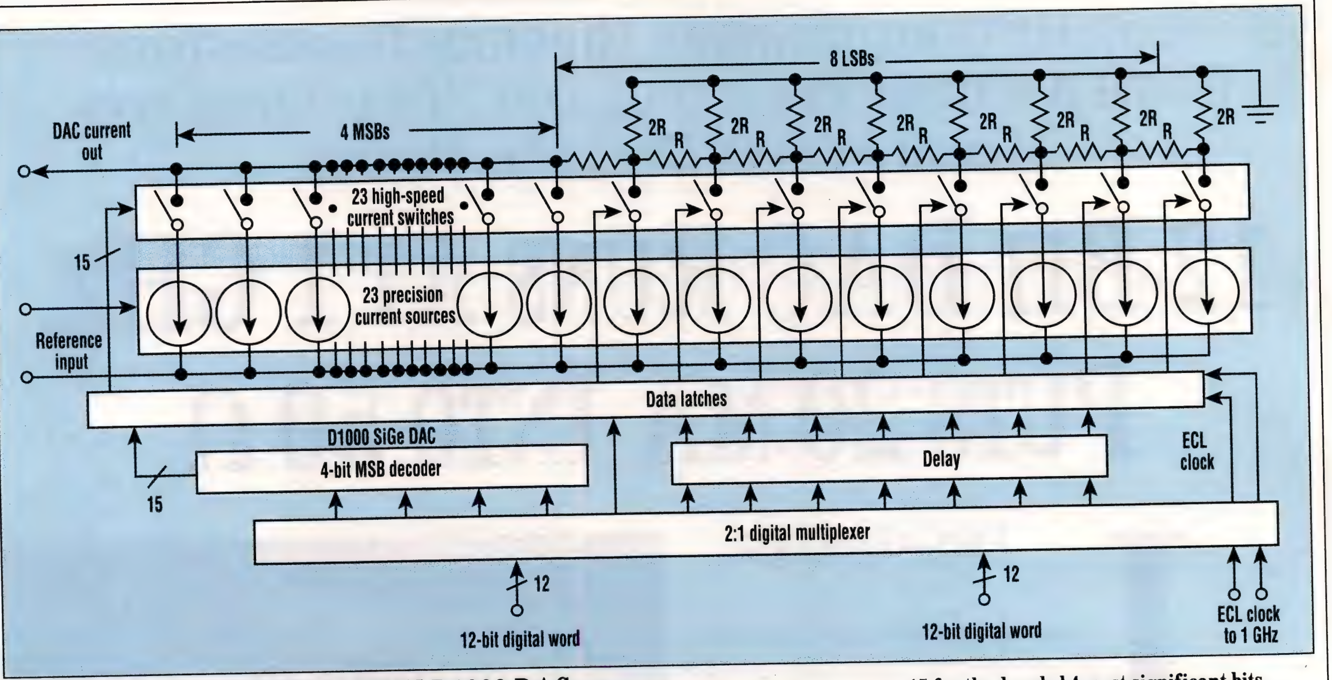
In an industry driven by rapid technology developments, it's easy to get jaded by endless announcements of faster, smaller, and cheaper ICs. But every so often, a technology appears that can truly be considered a "breakthrough." Such a breakthrough was evidenced at last December's International Electron Devices Meeting: IBM and Analog Devices announced their collaboration on applications for IBM's recently developed unique process that produces silicon-germanium (SiGe) heterojunction bipolar transistors (HBTs) (ELECTRONIC DESIGN, *Dec. 2, 1993, p. 48)*. Essentially, these HBTs reinvent bipolar semiconductor technology.

The transistors combine f_ts beyond 110 GHz with beta-Early-voltage (βV_A) products beyond 48,000. An earlier version of these transistors, which carried a lower combination of cut-off frequency and βV_A, provided Thomas Tice, Analog Devices' IC designer, with the device he needed to design a 12-bit current-output digital-to-analog converter (DAC). The new silicon-germanium DAC, which is the fastest to date, provides a new analog output at a frequency of 1 GHz but needs less than 1 W of power from a 5-V power-supply rail *(Fig. 1)*.

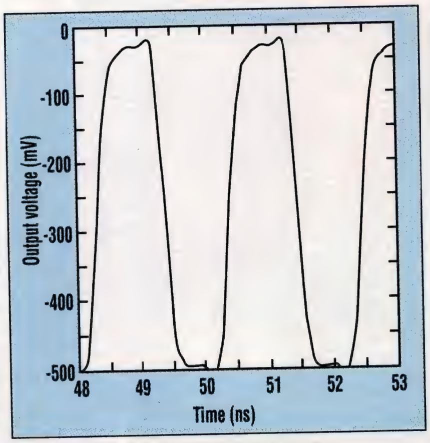


IBM fabricated the DAC on 8-in. wafers, using a process compatible with 0.25-μm CMOS. Called the D1000, the DAC's full-scale output current is 20 mA with a compliance voltage of one. That is, it can develop 1-V pulses across a load of 50 Ω with rise and fall times of less than 300 ps, or 500 mV across a load of 25 Ω *(Fig. 2)*. (Figure 2 is taken on a digital storage oscilloscope with an input impedance of 50 Ω. However, the DAC's output impedance, resulting from its R2R network, is also 50 Ω. Thus, the D1000's 20-mA output current only develops 500 mV across the oscilloscope's input.)

The performance of the D1000, a true IC built with 2854 SiGe npn HBTs and 1465 polysilicon resistors, is a function of the SiGe HBTs built on IBM's unique ultra-high-vacuum/chemical-vapor-deposition (UHV/CVD) process (ELECTRONIC DESIGN, *Jan. 10, p. 69)*. IBM built digital ICs on the process containing over 30,000 transistors. The story behind



1. THE SILICON-GERMANIUM D1000 DAC employs 23 precision current sources, 15 for the decoded 4 most-significant bits and 8 for the remaining 8 least-significant bits. The current sources drive an R2R ladder network. Toggling the 2:1 digital multiplexer on the DAC's input with an ECL clock permits switching the DAC's input word between any two codes at maximum speed.



2. WHEN THE SILICON-germanium DAC's input is toggled between all ones and all zeros at high speed, its 0-to-20-mA output produces a 500-mV signal across 25 Ω, with rise and fall times of about 300 ps.

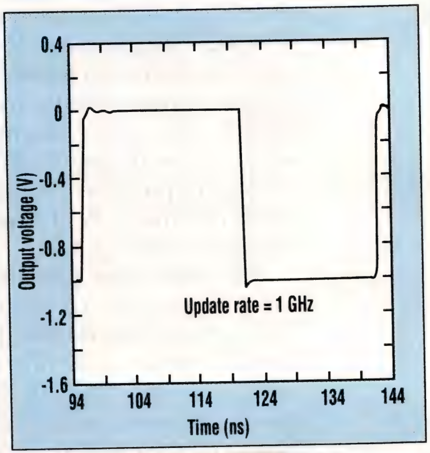
the development of the D1000, and its SiGe process, is as fascinating as the high-speed DAC and the process itself.

An IBM team led by Dr. Bernard Meyerson spent the last decade developing the UHV/CVD process at IBM's T.J. Watson Research Center, Yorktown Heights, N.Y., with major results coming over the last six years. However, during this time, the team's original goal of developing ultra-fast bipolar, digital transistors for supercomputer ICs died. Consequently, they felt the project had ended, because the massively parallel architectures made possible by the speed and density of submicron CMOS was deemed the way to go for higher supercomputer performance. Rather than kill the HBT project as the "old" IBM organization would have done, the IBM team recognized that their transistors offered added attributes for many analog applications. As a result, the IBM team contacted the process gurus at Analog Devices, forming what is now a two-year alliance.

BETA-V PRODUCT

In addition to their mind-boggling speed, the SiGe HBTs provide the analog designer with βV_A products several orders of magnitude greater than those of much slower silicon bipolar junction transistors (BJTs). The greater the βV_A product of a bipolar transistor, the better the current source that can be built with it. To that end, the D1000 uses at least 23 current sources: 15 for the four decoded most-significant bits (MSBs), and 8 for the remaining least-significant bits (LSBs) that drive a binary-weighted R2R network *(Fig. 1, again)*. Each of the 23 current sources consists of 8 separate current sources.

Work on the DAC, the first IC built with the SiGe HBTs, started about 15 months ago. The decision to build it was based on a very practical common-sense philosophy: Find out if these SiGe transistors really can be used to build high-performance analog ICs. Then build a 12-bit DAC with the available HBTs, and see how well it plays.



3. UPDATING THE D1000's digital input at 1 GHz yields a 1-V square wave across 50 Ω. Parasitics limit the maximum update rate.

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TVP3020

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Tom Tice of Analog Devices' Greensboro Group was given access to npn HBTs with an f_t of 46 GHz and a βV_A product of 1925. Rather than come up with a completely new design, he chose to emulate the architecture of the AD9712, Analog Devices' 100-MHz/12-bit current-output DAC which puts out a current of 20 mA. The AD9712 is built on a high-speed bipolar process with an f_t of about 3 GHz. Both DACs are ECL-compatible.

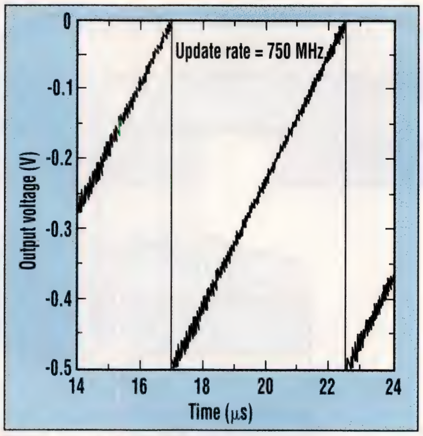
When the first wafers with their D1000 chips came out of the IBM fabrication facility, they were diced and mounted in ordinary ceramic 44-pin leaded packages (JLCC) with the knowledge that package and test-wiring parasitics would limit the DAC's performance. To ease the task of testing typical DAC parameters at high clock rates, a 12-line 2-to-1 digital multiplexer was built on the D1000's front end *(Fig. 1, again).*

At low speed (essentially dc), two different 12-bit words are applied to the digital multiplexer's pair of 12-line inputs. The digital multiplexer's 12 outputs (the DAC's 12 digital inputs) are toggled between the two input words at high clock rates. The two 12-bit input words can range from between any pair of adjacent LSBs and a swing from zero to full scale (form all ones to all zeros or vice versa).

The chip was hooked up and testing started at a frequency of 100 MHz. It worked, or as someone said, "it looked like a DAC," so the clock rate was raised to a frequency of 200 MHz. This process continued, increasing the clock rate 100 MHz at a time until it reached a frequency of 1 GHz *(Fig. 3).*

Beyond that frequency, the designers no longer had the required test equipment. The full 1-V output swing was developed across the 50-Ω source impedance and examined with a high-impedance oscilloscope probe.

The D1000's 1-GHz update-rate specification is based on the available test equipment, and could very well be faster. As a result, additional characterization is underway. The DAC's glitch-impulse is less than 5 pV-s, about the same as clock feedthrough when the data isn't changing.

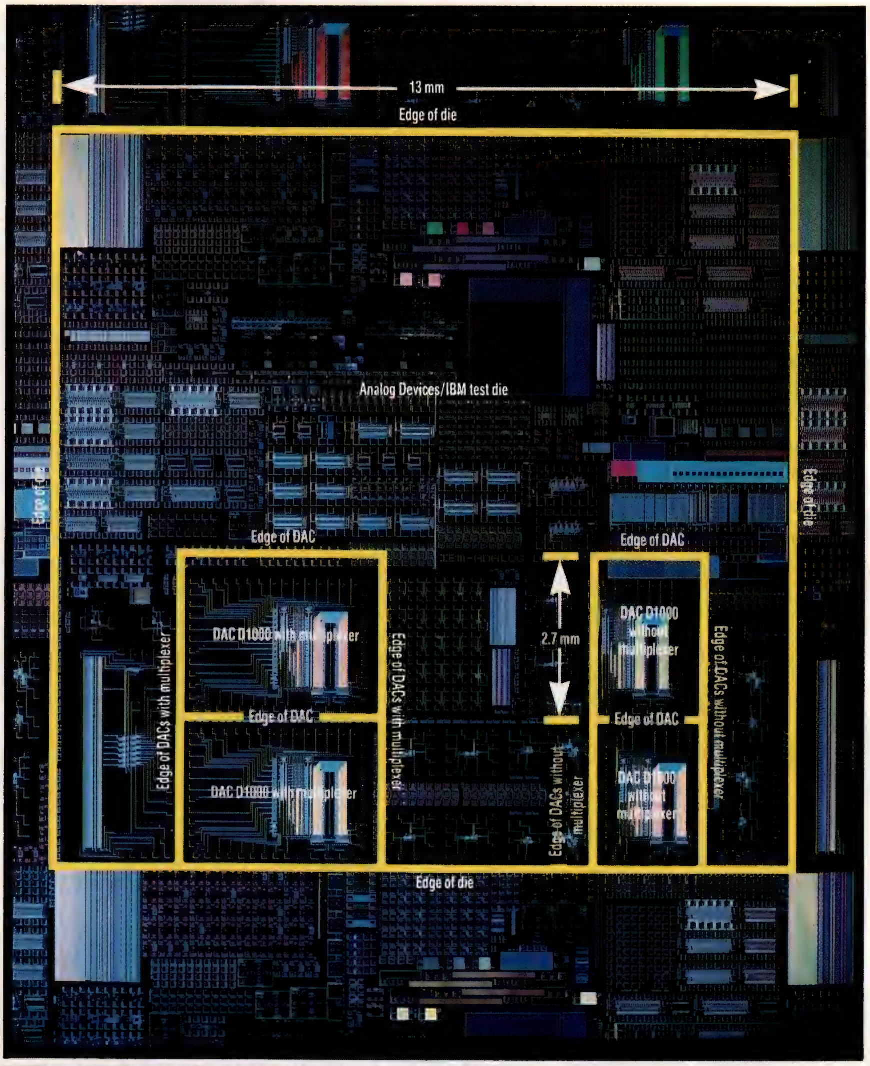


4. DRIVING ALL 12 bits of the D1000 directly from a 12-stage ECL counter running at 750 MHz will apply all 4096 codes to the digital input. This creates a ramp that confirms the DAC's ability to read every code.

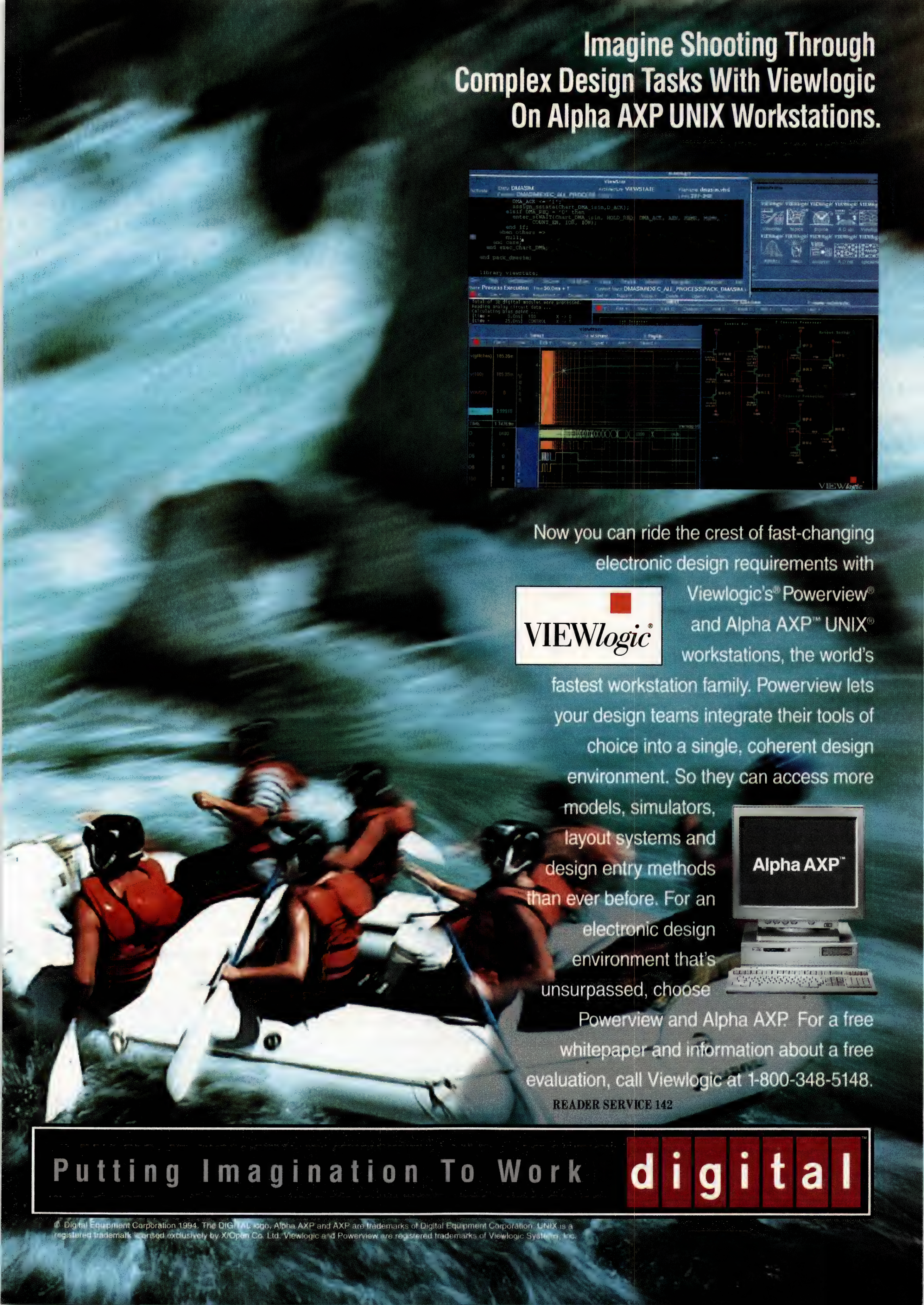
Driving the DAC directly (not using the multiplexer) from a 12-bit ECL counter running at a frequency of 750 MHz results in a ramp, confirming the DAC's ability to read all 4096 codes *(Fig. 4).*

Like most of today's high-resolution DACs and the silicon device it emulates, the SiGe D1000 combines segmentation of the MSBs with a binary-weighted R2R network for the LSBs. Both the 23 current sources and the 23 high-speed current switches (shown as mechanical switches in Figure 1) are constructed with the HBTs, on-chip ECL-compatible decoding and latching circuits, and 2:1 test-multiplexer circuits.

Unlike the device it emulates, the D1000 has neither a reference nor a reference-control op amp. Thus, off-


13 mm
Edge of die
Analog Devices/IBM test die
Edge of die
Edge of die
Edge of DAC
Edge of DAC
DAC D1000 with multiplexer
Edge of DAC
DAC D1000 with multiplexer
Edge of DACs with multiplexer
Edge of DACs with multiplexer
2.7 mm
DAC D1000 without multiplexer
Edge of DAC
DAC D1000 without multiplexer
Edge of DACs without multiplexer
Edge of DACs without multiplexer
Edge of die

5. THE PAIR OF TINY 12-BIT D1000 DACs (lower right) represent one of the many different analog devices built on a 13-mm^2 test die. Others include a pair of D1000s with a test multiplexer (lower left) and an ADC (lower-left corner).



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chip circuits are required. Developmental pnp transistors have been built on the process, however, so future HBT DACs can be made complete with references.

FIBER TO THE HOME

Any IC designer routinely using today's high-speed bipolar analog processes with their poor βV_A products knows the appliation in which they would like to use these HBTs. The same goes for the new UHV/CVD process that's used to build these devices.

For example, although the D1000 represents a "technology demonstration" and immediate applications for it weren't expected, it has already found a niche to fill—fiber-to-the-home links in Eastern European countries. In this area of the world, the telephone infrastructure is being done over literally from the ground up. The HBT DACs will be located at the end of the glass fiber line where they will convert a high-frequency digital signal, encoded with TV, voice, and data, to a frequency-division-multiplexed analog signal. In this application, DACs will be used in die form in a multichip module (MCM). As a result, package and chip interconnection parasitics will be at a minimum.

The D1000 should also find applications in direct-digital synthesis (DDS), where it can create modulated high-frequency (RF) sine waves for receivers and transmitters from digital words. DDS, which represents the major application for the 100-MHz AD9712 (which the SiGe DAC emulates), is suitable particularly in spread-spectrum and other digital RF communication applications. The D1000 should prove useful at frequencies from 100 MHz and up. At lower frequencies, package parasitics will be less of a problem.

PURE RF

The SiGe process not only lends itself to RF applications in devices like this DAC, but it should also find homes in a number of pure RF applications now served by gallium-arsenide (GaAs) devices. These include RF amplifiers, modulators, and demodulators in transmitters and/or receivers for cellular and cordless telephones, as well as other present and upcoming consumer products. As a result, Analog Devices formed a group within the company expressly for the design and marketing of such ICs (ELECTRONIC DESIGN, *Dec. 2, 1993, p. 14 and p. 28).*

The size of the D1000 die relative to the size of typical die from its process indicates the degree of advancement the process brings to the analog arena. As noted earlier, the D1000 is built on 8-in. wafers designed to build 0.25-μm CMOS ICs of thumbnail size as well as larger-size die.

Most semiconductor companies use what they call test wafers for developmental chips. Each wafer contains multiples of a number of different ICs rather than just one IC. However, the analog die (and IBM test devices) are so small that Analog devices and IBM are using test die that each contain multiple ICs *(Fig. 5).* This joint Analog Devices/IBM test die is 13 mm on a side with virtually all devices in the lower half designed by Analog Devices.

The DAC1000 without the multiplexer (lower right) is a mere 2 by 2.7 mm. The D1000 with the multiplexer (lower left) is about twice that size. The open area on the die, to the left of the DAC, contains the 24 input lines to the multiplexer. The test die also contains an ADC, half a dozen comparators, several RF ICs, a transistor array, and a number of ECL circuits. The comparators take about a quarter of the area required by the D1000 *without* the multiplexer, and the RF ICs take about one third the area. The individual ICs are cut from the die with a saw.☐

PRICE AND AVAILABILITY

The SiGe D1000 is only available in die form. For additional information concerning price and availability, call Tom Gratzek at (910) 605-4233.

Analog Devices Inc., 7910 Triad Center Dr., Greensboro, NC 27409; (910) 605-4233.

For information on RF applications for the SiGe HBTs, call Doug Grant at (617) 937-1481.

Analog Devices Inc., 181 Ballardvale St., Wilmington, MA 01887-1024; (617) 937-1481.

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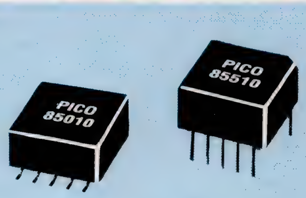

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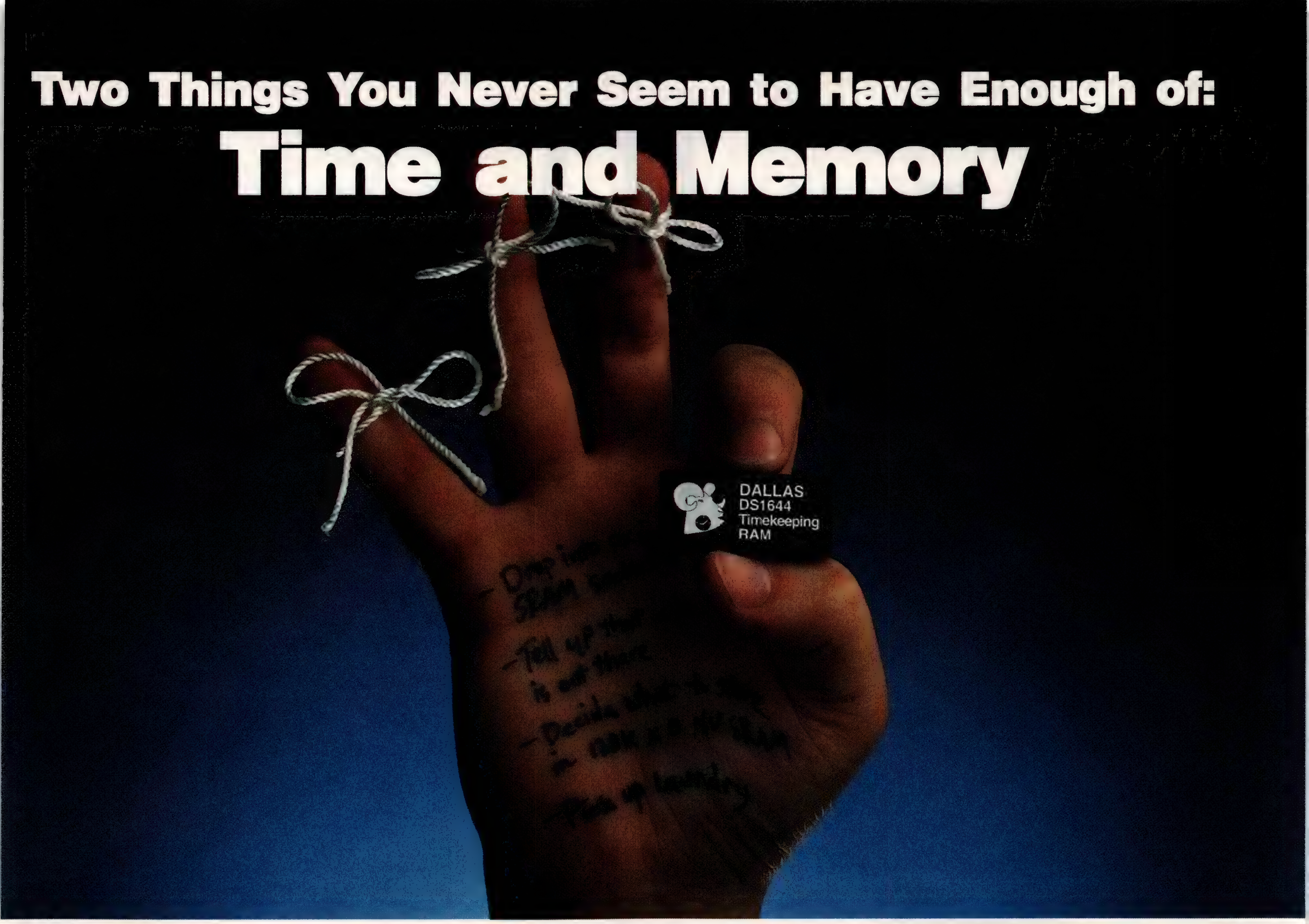

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DS1644	32K x 8	28-Pin Encapsulated DIP	**Nothing, Zip, Nada. Nobody else offers densities this high.**
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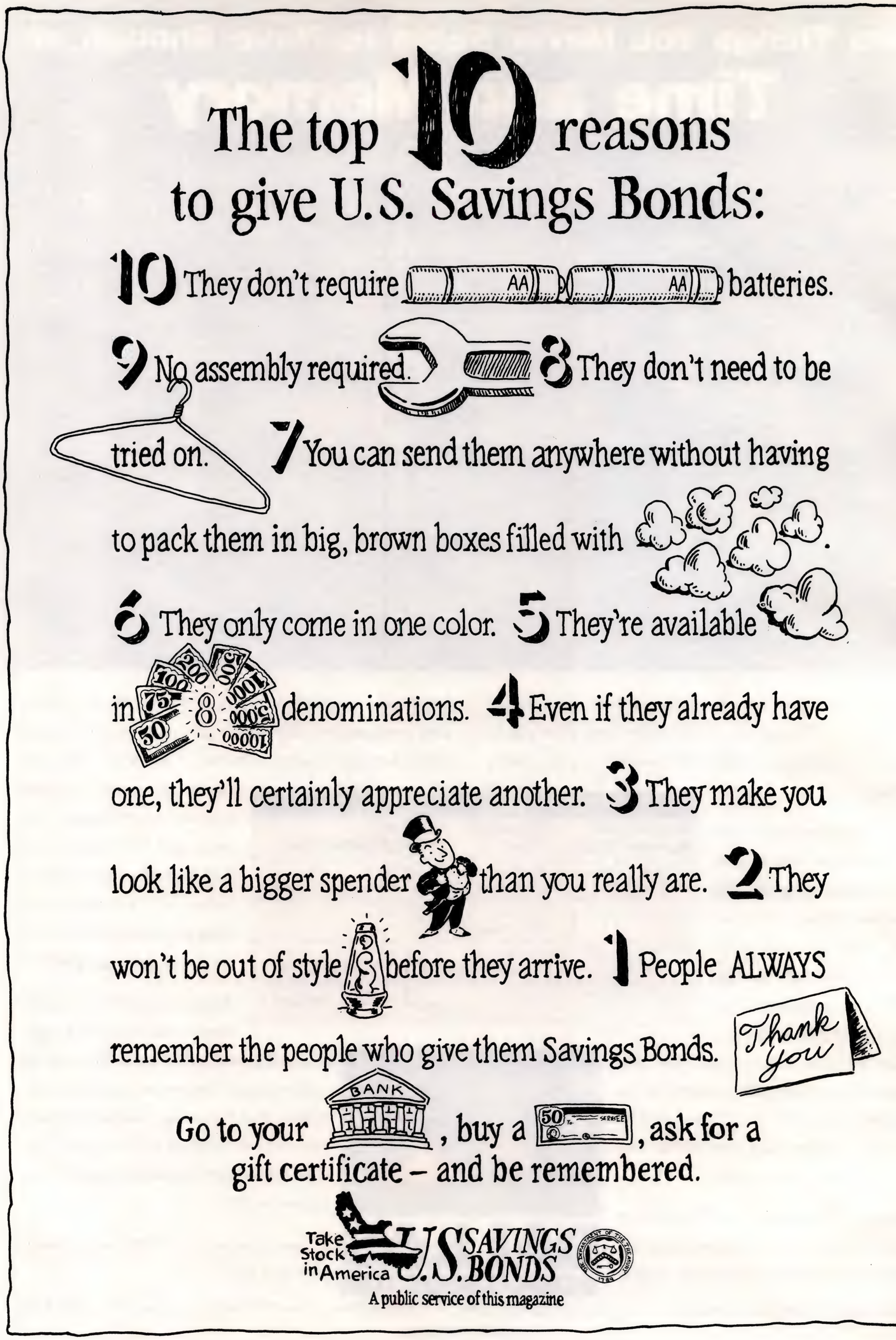

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THE PROPER CHOICE OF ALGORITHMS AND EFFICIENT MAPPING ARE KEY TO SQUEEZING PERFORMANCE FROM MULTIPROCESSOR CHIPS AND BOARDS.

HARNESS MULTIPROCESSING POWER FOR DSP SYSTEMS

While single-processor digital signal processors are the computational engines for such applications as disk controllers, cellular telephones, and consumer devices, even greater speed and more challenging applications can be addressed with the power of multiprocessor digital-signal-processing (DSP) chips and boards. Actually, the computational power available from DSP implementations increases with integration, from single-processor chips, to multiprocessor boards, to multiprocessor chips and boards. However, the key to exploiting this power is properly selecting and mapping algorithms.

Significant performance increases in signal processing can be achieved with algorithms that are tailored to multiprocessor implementations. For example, on a multiprocessor system, the Fourier transform can be implemented in O(N) cycles, in contrast to single-processor implementations that are $O(N \times N)$, or $O(N \times \log N)$ at best. Also, convolving, or FIR filtering, of multiple sections of a signal can occur simultaneously. Dynamic time warping, the frequent nemesis of rapid signal processing, takes place at high speed using parallel computation. Signal classification employing popular template matching techniques can be performed simply and quickly by delegating the various template vectors to different processors and broadcasting the unknown vector to be identified. Most importantly, multiprocessors can perform an entire sequence of computations that compose a total solution. For instance, spectral processing transforms the signal from the time-amplitude domain to the frequency-decibel domain.

This article will use the CNAPS chip from Adaptive Solutions to illustrate the principles behind mapping DSP algorithms to multiple processors. The multiprocessor CNAPS provides 64 processors on a 1-in.^{2} chip. Each individual processor functions as a digital signal processor performing 16-bit, fixed-point arithmetic at 20 MHz, which is an aggregate potential equivalent to a single-processor performing at 1280 MHz.

The computations performed are orchestrated within a SIMD architecture, in which the same sequence of instructions is executed on different sets of data. A single program broadcasts the same sequence of instructions to each processor, which in turn operate on the unique data in their distributed memories *(Fig. 1)*. Common data (typically a second operand) can be broadcast from a shared

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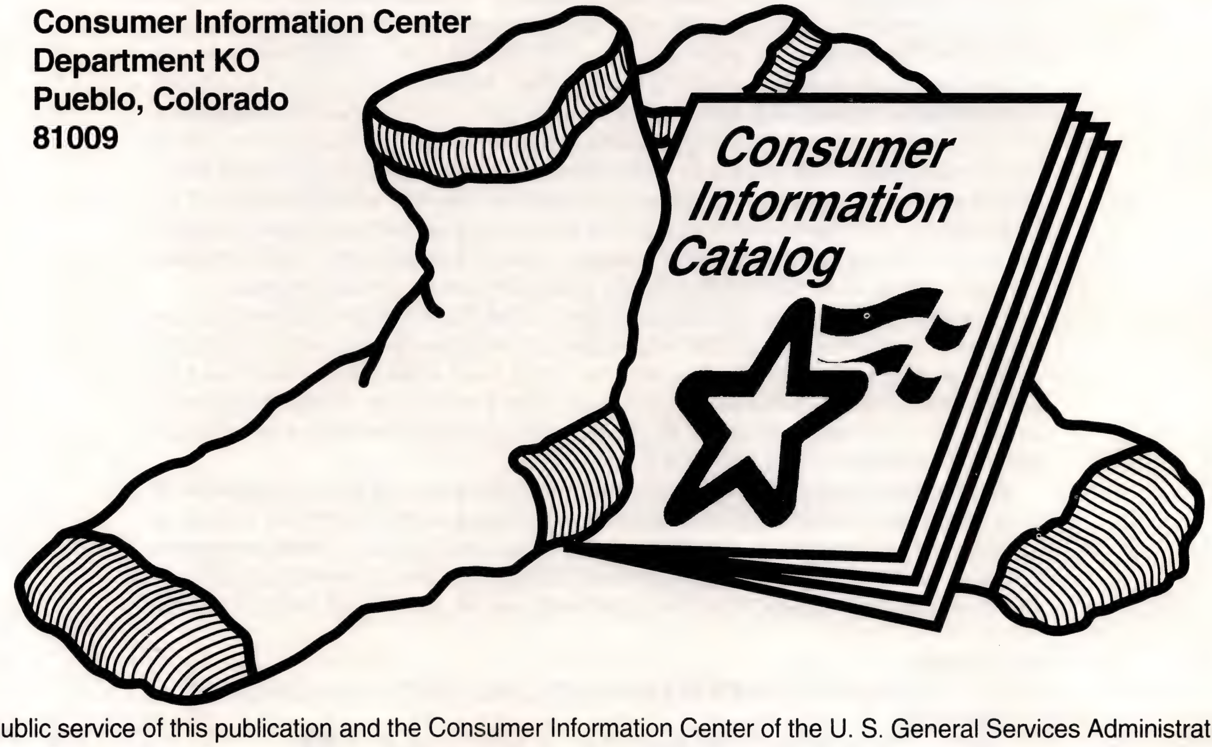

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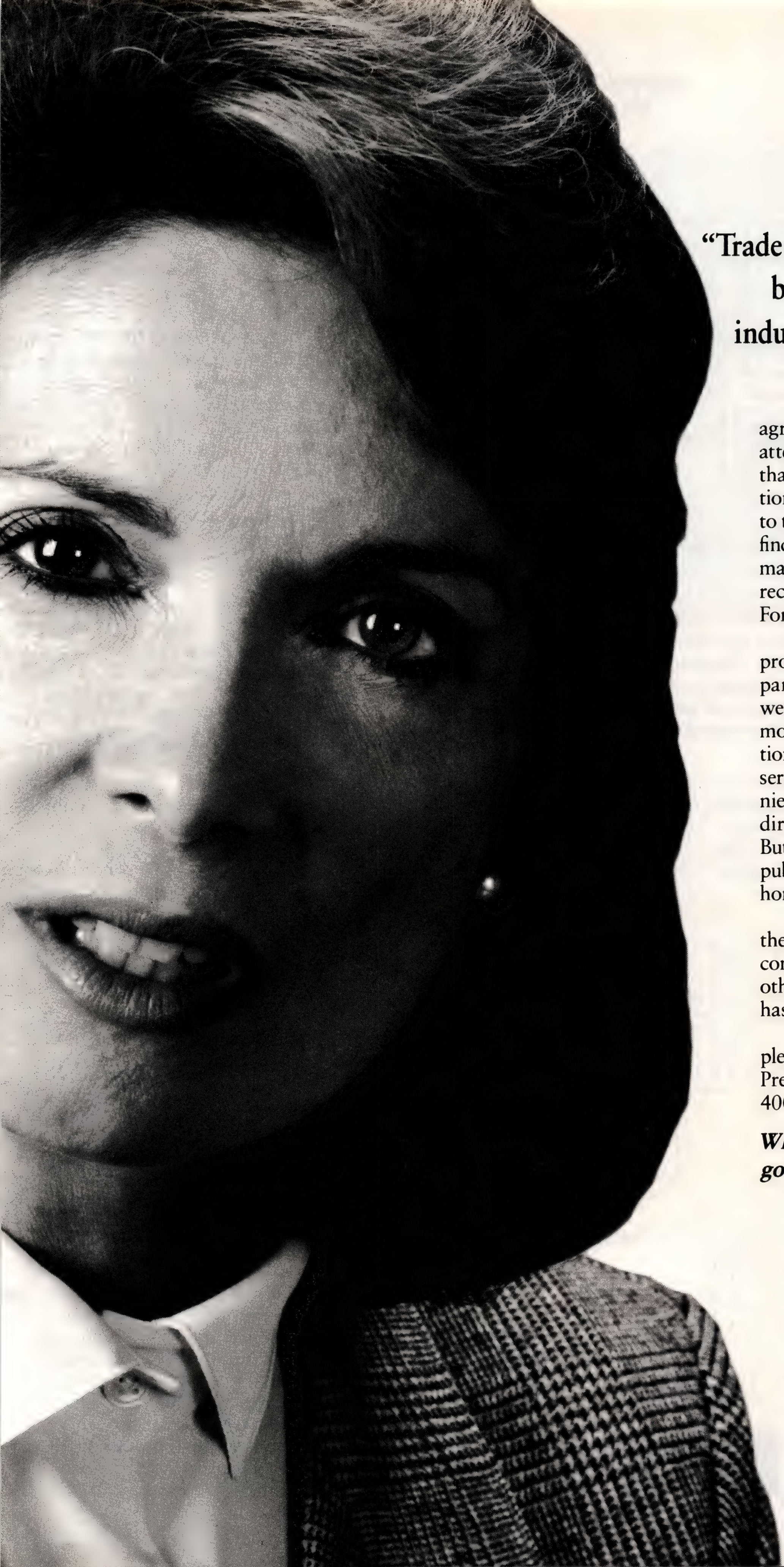

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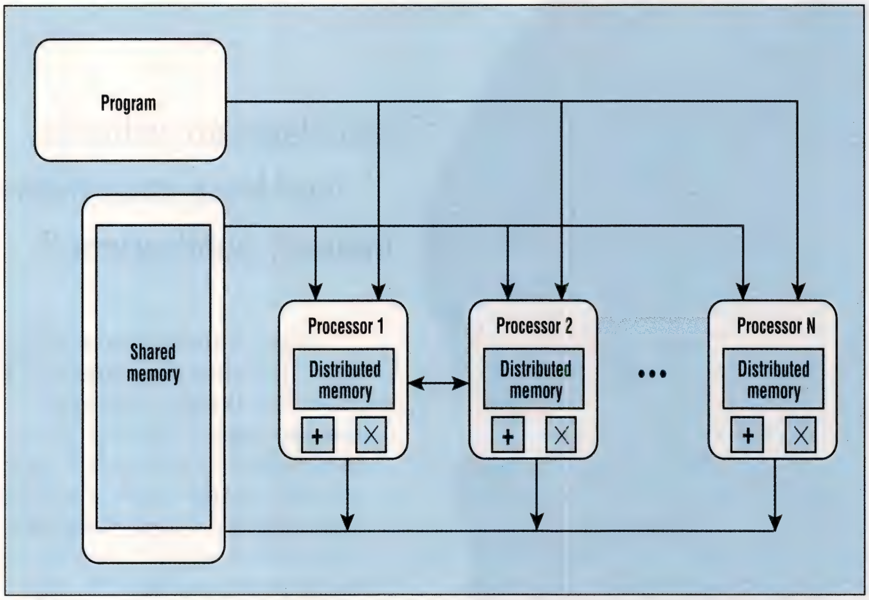
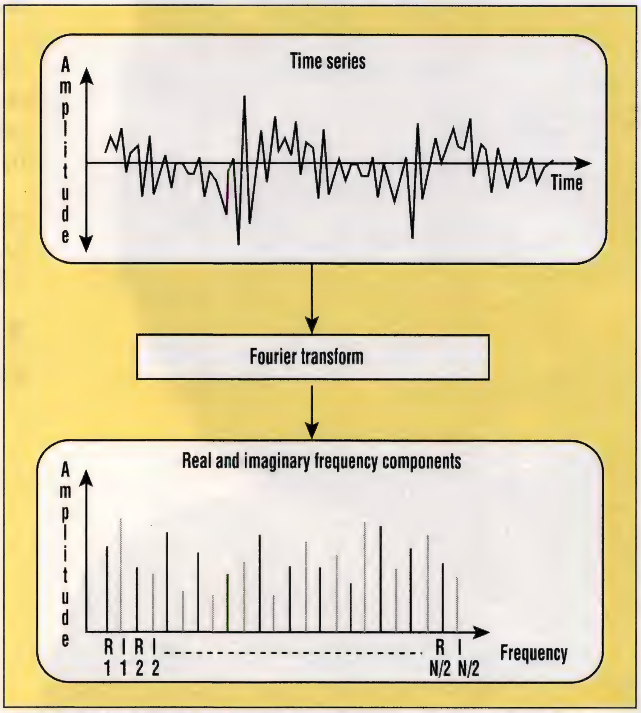


1. THE CNAPS MULTIPROCESSOR architecture combines 64 processors on a 1-in.^{2} chip. Each individual processor functions as a digital signal processor performing 16-bit, fixed-point arithmetic at 20 MHz. This is potentially equivalent to a single processor performing at 1280 MHz. A single program broadcasts the same sequence of instructions to each processor, which in turn operate on the unique data in their distributed memories. It also can broadcast common data from a shared memory to all of the processors.

memory to all of the processors. In addition, data in adjacent processors can be exchanged via a nearest-neighbor connection. Implicit in this SIMD architecture is a unified programming model that naturally integrates the power of the multiple processors. Boards containing multiple CNAPS chips can transparently extend the SIMD structure to a total of 8 chips, or 512 processors—the performance potential equivalent to a single-processor operating at 10 GHz.



2. FREQUENCY analysis typically employs the Fourier transform, an algorithm that determines the frequency components of a function originating in the time domain.

Harnessing the power of multiple processors requires the proper selection of algorithms and appropriate mapping of the algorithms to the target architecture. The original matrix-vector multiply formulation of the Fourier transform more efficiently fits a multiprocessor system than does the fast-Fourier-transform workhorse that was designed for traditional single processors. Selecting algorithms for solving systems of equations, either iteratively (Jacobi vs. Gauss-Seidel) or directly (Gauss-Jordan Elimination vs. Gaussian-Elimination), requires a similar revisitation of algorithm choices. The goal is to minimize interprocessor dependencies while maximizing the use of the computational resources.

The primary areas of signal processing include: frequency analysis, filtering, linear predictive coding, dynamic time warping, and classification. The following sections describe the mapping of the principal algorithm in each of these areas to the CNAPS multiprocessor. Maximum efficiency is achieved when an integrated sequence of algorithms is performed on the multiprocessor DSP system.

The standard algorithm used to determine the real and imaginary frequency components of a time series is the Fourier transform *(Fig. 2)*. As originally formulated, the algorithm is a matrix-vector multiply. The rows of the matrix are cosine and sine functions, and the number of periods in these functions increases with the row number in the matrix. Multiplying the time-series vector by the matrix produces a set of correlations, resulting in the corresponding frequency-composition vector. While conceptually straightforward, the matrix-vector computation is $O(N \times N)$ for a single-processor implementation. In 1969, Cooley and Tukey, noting the pattern of values in the cosine-sine matrix, formulated the fast Fourier transform, an iterative process that reduces the single-processor computation to $O(N \times \log N)$.[1]

On the CNAPS multiprocessor system, the algorithm of choice for computing reasonably-sized Fourier transforms is the original matrix-vector multiply formulation. Each row of the cosine-sine matrix is loaded on a different processor *(Fig. 3)*. The time series elements are then broadcast sequentially. The inner-products corresponding to the individual real and imaginary frequency components are computed concurrently using the single, broadcasted program. Reverting to the straightforward formulation of the

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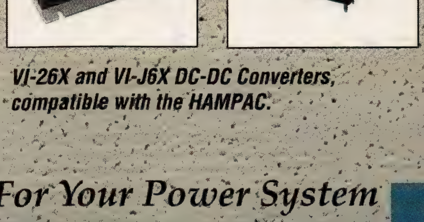

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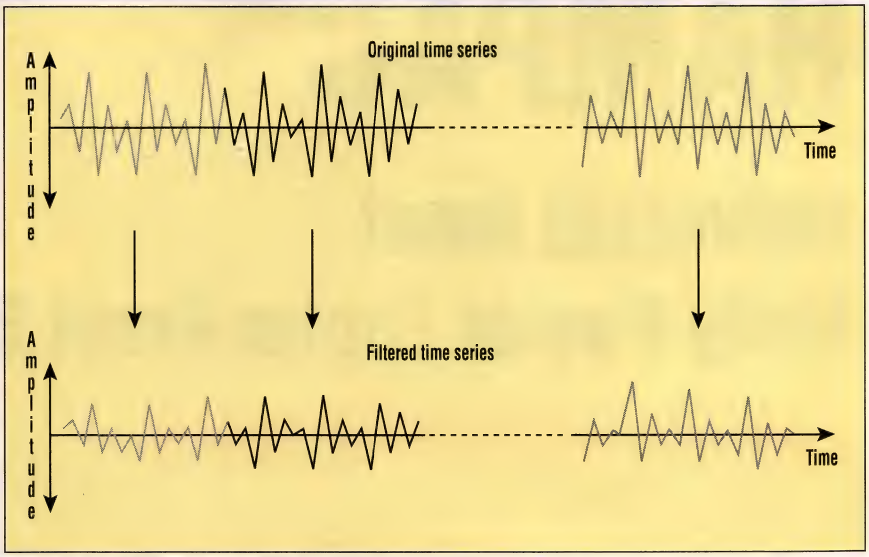
Fourier transform algorithm avoids the loss of precision inherent in the iterative technique, and reduces the computation to only O(N).

Using one CNAPS chip (64 processors), the matrix-vector algorithm can compute a 32-sample complex Fourier transform in O(32) multiply-accumulates, as opposed to O(32 × 5) for the most efficient single-processor solution. Thus, even if the clock speed of the single processor is double that of the multiprocessor, the latter solution is still more than twice as fast.

A finite-impulse-response (FIR) filter is simply a convolution of a time series with a vector of weights. For example, if the value of each of the weights is 1/N, then the computation is equivalent to a moving-average, low-pass filter.

On a multiprocessor system, multiple sections of a time series can be filtered concurrently *(Fig. 4)*. Vectors corresponding to separate sections of a time series are first loaded onto different processors *(Fig. 5)*. The vector of filter weights is then broadcast sequentially to each of the processors, which are multiplied by the corresponding time-series elements according to the single program. Finally, the final inner-product sum is the new element value in the resultant, filtered time-series sections. This process of broadcasting the filter weight vector and computing the resulting inner-product is repeated for each element to be filtered in the time-series sections.

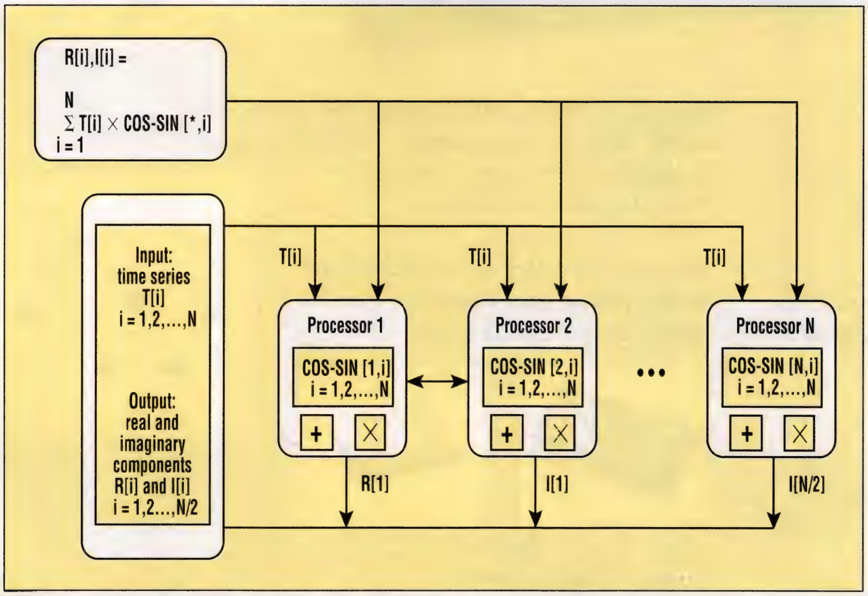


4. A FINITE IMPULSE RESPONSE (FIR) filter is simply a convolution of a time series with a vector of weights.

Using the CNAPS multiprocessor implementation, an O(M1 × M2 × N) process is accomplished with only O(M1 × M2) computations. For example, 500 processors (with filter length 10) can filter 500 times-series sections of length 100 with 1000 multiply-add operations. The same task takes 500,000 multiply-add operations on a single processor. Consequently, the filtering is performed 200 times faster on a 20-MHz, 512-processor system than it would be on a 50-MHz single-processor DSP implementation.

Linear predictive coding of signals has proven to be a useful technique for a variety of applications, originally in geophysics and more recently in economics and speech processing. Conceptually, the motivation is to predict the (i+1) element of a time series from a linear combination of the previous p samples of the series. Other motivations include smooth (all-pole) modeling of frequency responses and efficient, narrow-bandwidth encoding.

The basic computations include autocorrelation of the time series, formation of a linear system of equations from the autocorrelation coefficients, and solving that system for the predictor coefficients. The autocorrelation portion can be efficiently accomplished on a multiprocessor system by simply broadcasting the time series to the distributed memories of a sequence of processors, and allowing for a one-element delay in the portion of the time series that's received by the sequential processors. The original time series is then rebroadcast in its entirety, and a different element of the resulting autocorrelation vector is simultaneously



3. WHILE THE FAST FOURIER algorithm works best for single-processor DSP systems, a multiprocessor system's algorithm of choice for computing reasonably sized Fourier transforms is the original matrix-vector multiply formulation. Each row of the cosine-sine matrix is loaded on a different processor. The time-series elements are then broadcast sequentially to obtain the real and imaginary components.

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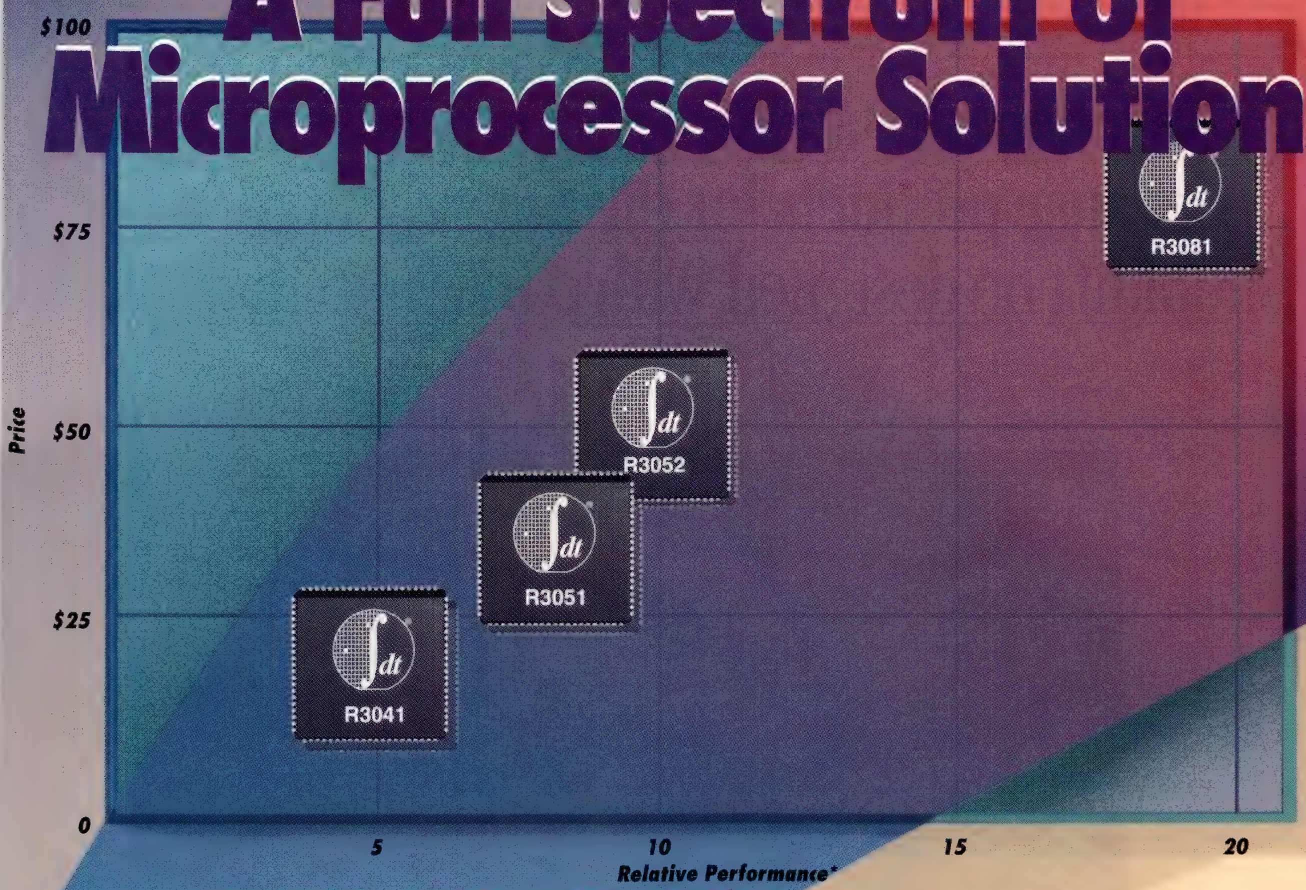

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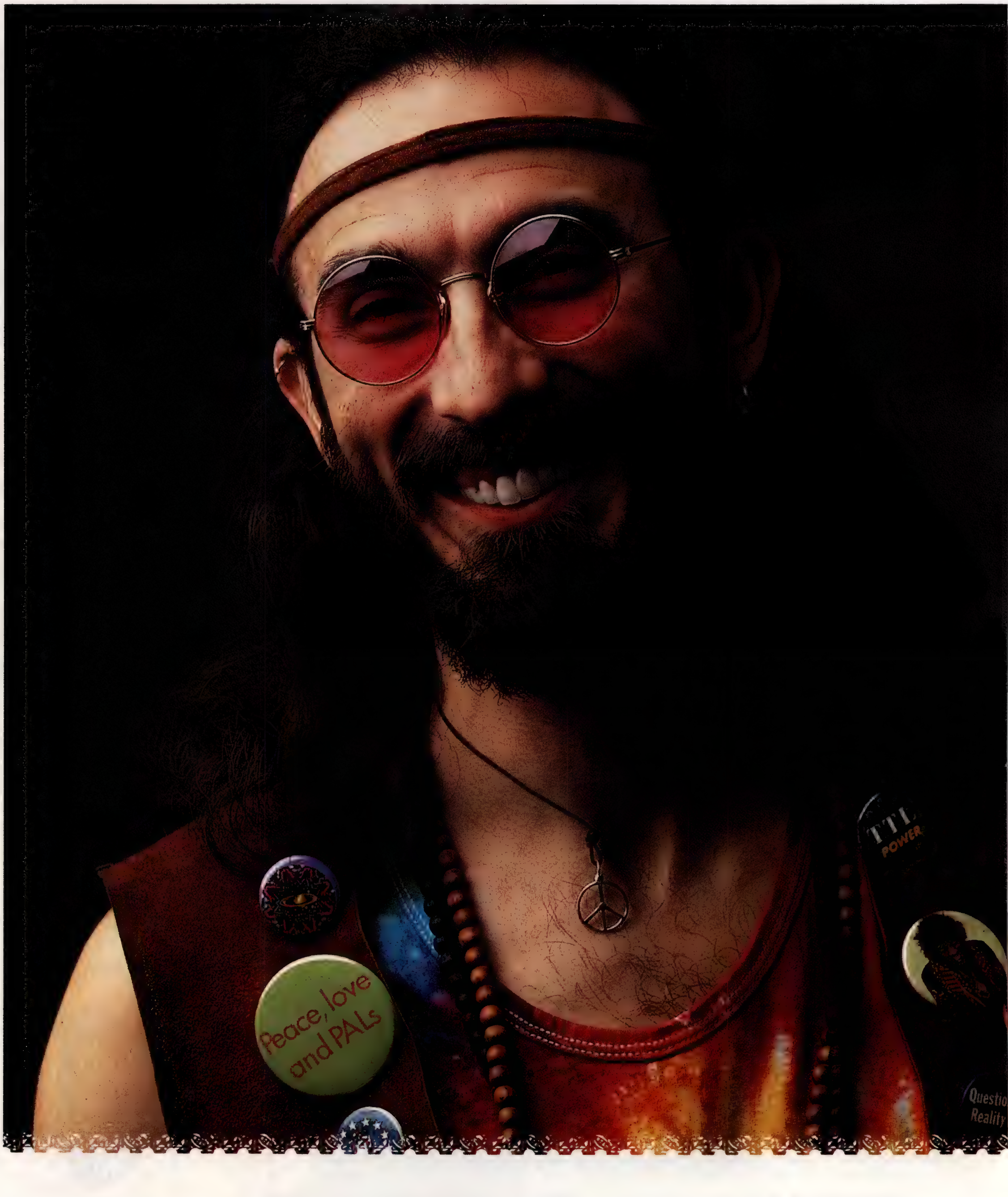

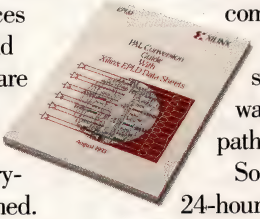
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computed as an inner-product on each processor.

To solve the small linear system of equations (typically of order 20 or less), Gauss-Jordan Elimination would be a prudent algorithm choice to implement on a multiprocessor system. Interprocessor communication is minimized and multiple processor activity is maximized. In the Gauss-Jordan technique, all of the off-diagonal elements are eliminated, avoiding the back-substitution computation required in standard Gaussian Elimination. It yields a matrix and vector that require only one division computation for each element to produce the solution vector *(Fig. 6)*.

In mapping the Gauss-Jordan solver to the multiprocessor CNAPS system, one column of the coefficient matrix A[i,j] is loaded into the memory of each of the first N processors, and the coefficient vector B[i] is loaded in the memory of the (N+1) processor *(Fig. 7)*. To maintain consistency, the right-hand-side of the system of equations (the B[i] vector loaded in the (N+1) processor) must undergo the same algebraic manipulations as the A[i,j] matrix.

Distributed across the multiple processors is the multiplication of each element in a matrix row by a scalar elimination coefficient. In addition, the resulting values are added to the corresponding elements in the row of the matrix containing the element to be eliminated. Depending upon which element of the matrix is currently being eliminated, one of the processors computes the elimination coefficient E and broadcasts it to all of the other processors. They, in turn, use the elimination coefficient as the scalar multiplier for their respective row element. After the matrix is completely diagonalized, the resulting N values in the (N+1) processor's B[i] vector become the respective divisors for the diagonal elements in the first N processors. This results in the solution vector, which has one element per processor.

In performing the elimination process for solving a system of equations on N+1 processors, only N/2 of the processors, on average, are actively participating in the computations. Thus, the multiprocessor speed advantage isn't as dramatic as for other computations. However, when required as part of a total application, the solution of a modest linear system of equations is practical and contributes to the speed of the overall solution.

$$\begin{bmatrix} A[1,1] & A[1,2] & A[1,3] & A[1,4] \\ \boxed{A[2,1]} & A[2,2] & A[2,3] & A[2,4] \\ A[3,1] & A[3,2] & A[3,3] & A[3,4] \\ A[4,1] & A[4,2] & A[4,3] & A[4,4] \end{bmatrix} \times \begin{bmatrix} X[1] \\ X[2] \\ X[3] \\ X[4] \end{bmatrix} = \begin{bmatrix} B[1] \\ B[2] \\ B[3] \\ B[4] \end{bmatrix}$$

For example,
Gauss-Jordan elimination of element A[2,1]:

$$E = -A[2,1]/A[1,1]$$

$$A[2,J] = A[2,J] + A[1,J] \times E$$

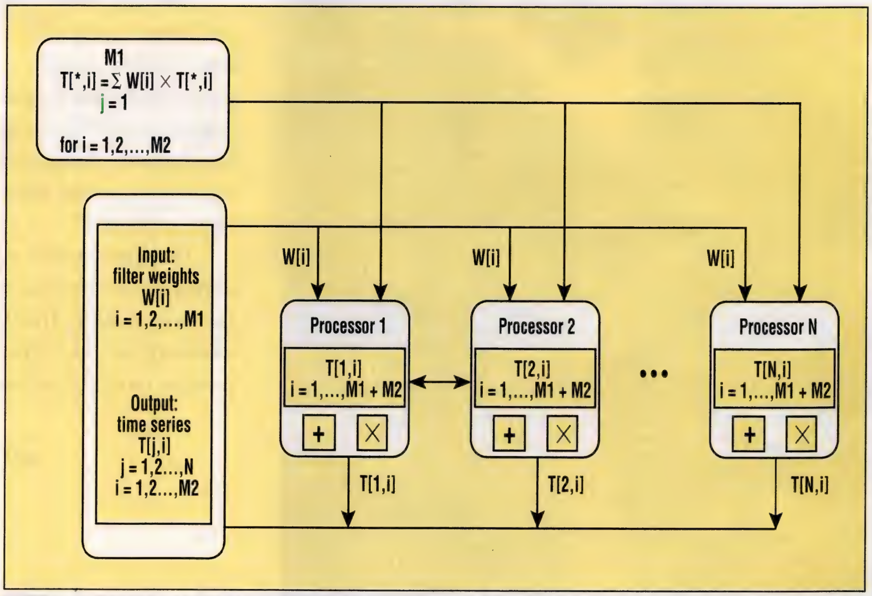
$$\text{for } J = 1,..,4$$

$$B[2] = B[2] + B[1] \times E$$

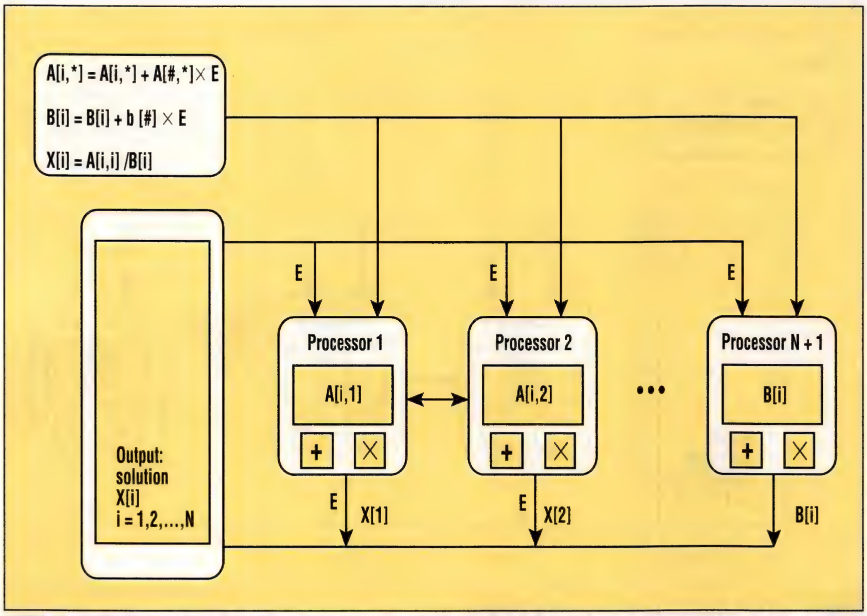
6. THE BASIC computations for linear-equation solving include autocorrelation of the time series, formation of a linear system of equations from the autocorrelation coefficients, and solving that system for the predictor coefficients. Gauss-Jordan elimination is satisfactory in determining a small linear system of equations. In the Gauss-Jordan technique, all of the off-diagonal elements are eliminated, avoiding the back-substitution computation required in standard Gaussian elimination. The resulting matrix and vector require only one division computation for each element to produce the solution vector.

Dynamic time warping is a process that determines the warping function for aligning two semantically equivalent time series featuring unique, nonlinearly aligned time patterns *(Fig. 8)*. The process proceeds by first breaking each of the time series into a sequence of short-duration units. Each unit is then characterized by a feature vector, such as the relative amplitudes of the frequency components that represent the composition of the unit of time.

A matrix is then formed by placing the sequence of feature vectors representing each of the time series on orthogonal dimensions of the matrix. The matrix should be populated with the Euclidean distances between the feature vectors corresponding to the node intersections in the matrix. The ideal warping pat-



5. WHEN CONVOLUTION IS PERFORMED on a multiprocessor system, multiple sections of a time series can be filtered concurrently. Vectors corresponding to separate sections of a time series are first loaded onto different processors. The vector of filter weights is then broadcast sequentially to each of the processors, and they are multiplied by the corresponding time-series elements according to the single program.



7. WHEN MAPPING THE GAUSS-JORDAN solver to the multiprocessor CNAPS system, one column of the coefficient matrix A [i,j] is loaded into the memory of each of the first N processors, and the coefficient vector B [i] is loaded in the memory of the (N + 1) processor. The process of multiplying each element in a matrix row by a scalar elimination coefficient is distributed across the processors.

tern for nonlinearly aligning the two time series is determined by the minimum total Euclidean distance path to transverse the matrix nodes, from the bottom left to the top right (subject to the algorithmically-limited options available for reaching any particular node). In the staggered-array algorithm, the options for reaching node [i,j] are from either node [i-1,j-2] or from node [i-2,j-1]. The node with the minimum accumulated distance is selected, and that distance is added to the Euclidean distance for node [i,j]. This becomes the accumulated total distance for node [i,j].

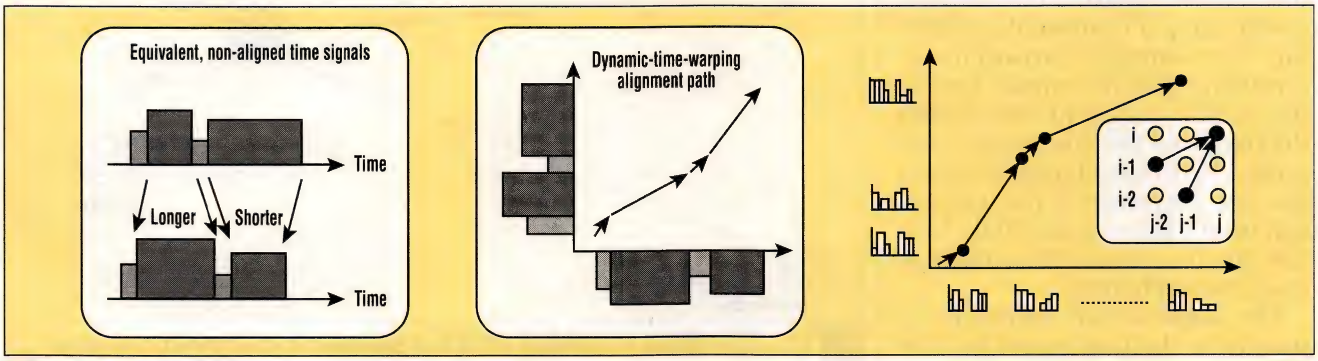
A multiprocessor DSP system can efficiently compute the feature vectors, for example, as frequency components. Furthermore, the matrix of Euclidean distances can be computed an order-of-magnitude faster on a multiprocessor system than on a single-processor system. This is done by first loading the feature vectors for one of the time series on successive processors. Then, the system sequentially broadcasts the feature vectors from the other time series, and concurrently computes an entire row of Euclidean distances as each feature vector is broadcast.

Transversing the matrix to determine the warping function that ideally aligns the two time series also can be performed using a multiprocessor system *(Fig. 9)*. Following the concurrent computation of the Euclidean distances, each successive processor calculates a column of the matrix. The computation proceeds by computing the accumulated distances for each node in an entire row, all at the same time.

To perform the required computation, each node [i,j] in a row needs the accumulated distances from relative nodes [i-1,j-2] and [i-2,j-1]. This can be easily transmitted using the nearest-neighbor connection between adjoining processors. Due to the regularity of the process, all nodes perform this relay of information concurrently. Each processor then independently determines the minimum of its two inputs, adding that minimum to its Euclidean distance to yield the accumulated distance for its node in the matrix. After performing this same concurrent computation on each successive row, terminating with the top row, the ideal path is declared to be the one with the minimum accumulated distance in the top row, subject to normalization for path length. The multiprocessor CNAPS chip can use the nearest-neighbor connection to optimize the reduction operation to determine the minimum.

TIME WARPING

The single-processor version of dynamic time warping is an irregular process—it seeks to prune the computation while transversing the matrix. This is done to minimize computation, perhaps at the expense of missing the optimal warping path. Successful mapping of the dynamic-time-warping algorithm to a multiprocessor system involves maintain-


Equivalent, non-aligned time signals
Time
Longer
Shorter
Time
Dynamic-time-warping alignment path
i
i-1
i-2
j-2
j-1
j

8. DYNAMIC TIME warping is a process that determines the function needed to align two time series. Each of the time series is broken into a sequence of units characterized by feature vectors. These vectors form a matrix that's filled with the Euclidean distances between the vectors. The warping funcOion is then determined as the minimum path of accumulated Euclidean distances in transversing the matrix.

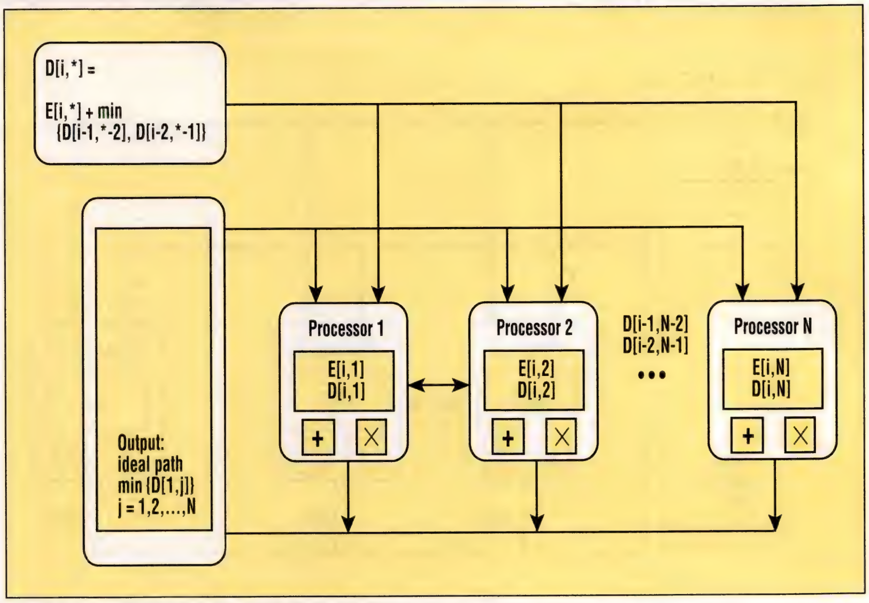
ing a regularity in the computations required of each processor. This capitalizes on the ability of multiple processors to concurrently compute all possible alignment paths.

The most common form of classification is multi-template matching. Each template is defined by a feature vector in M-dimensional space. The identity of an unknown vector to be classified is defined to be the closest match in the M-dimensional space, as determined by the minimum Euclidean distance *(Fig. 10)*.

A multiprocessor is the ideal computational resource for performing this type of classification. Each template feature vector (TP[i,j]) is loaded into the memory of a different processor *(Fig. 11)*. The unknown feature vector (UKN[j]) is then broadcast from the shared memory to all of the processors, which compute the N Euclidean distances (ED[i]) concurrently. The classification of the unknown feature vector corresponds to the processor having the minimum Euclidean distance.

In a recent test, a 256-processor 6U VME CNAPS board was shown to be over 100 times faster than a single-processor solution when performing this type of algorithm for the signal-processing application of optical character recognition.

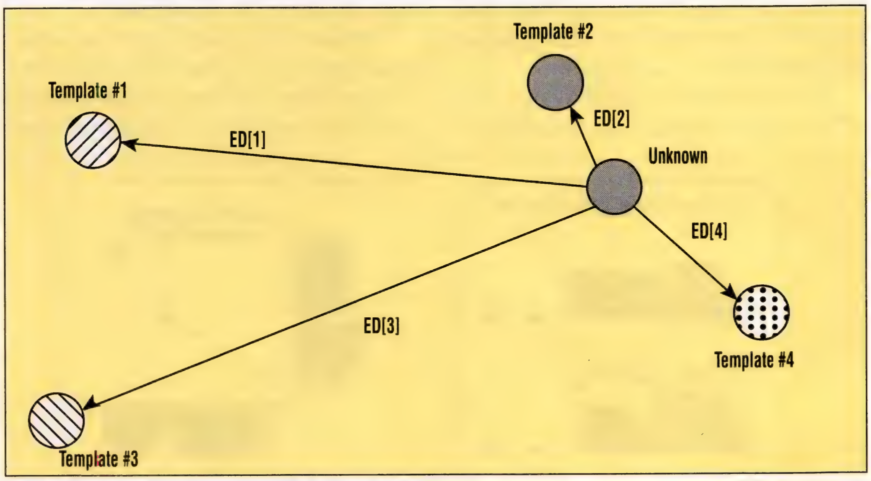
For maximum efficiency, an entire application that encompasses a sequence of computations must be performed on the multiprocessor. This amortizes the time involved in loading and unloading data to and from the distributed memories and the shared memory. Moreover, it's essential to ensure that the sequence of operations comprising a total solution can be mapped to the multiprocessor using a common data structure. This minimizes the need for unproductive data movement. Earlier, this article discussed determining the frequency composition of a time series. That computation is usually just one component in the transformation of a time-vs.-amplitude function into its corresponding frequency-vs.-decibel function.



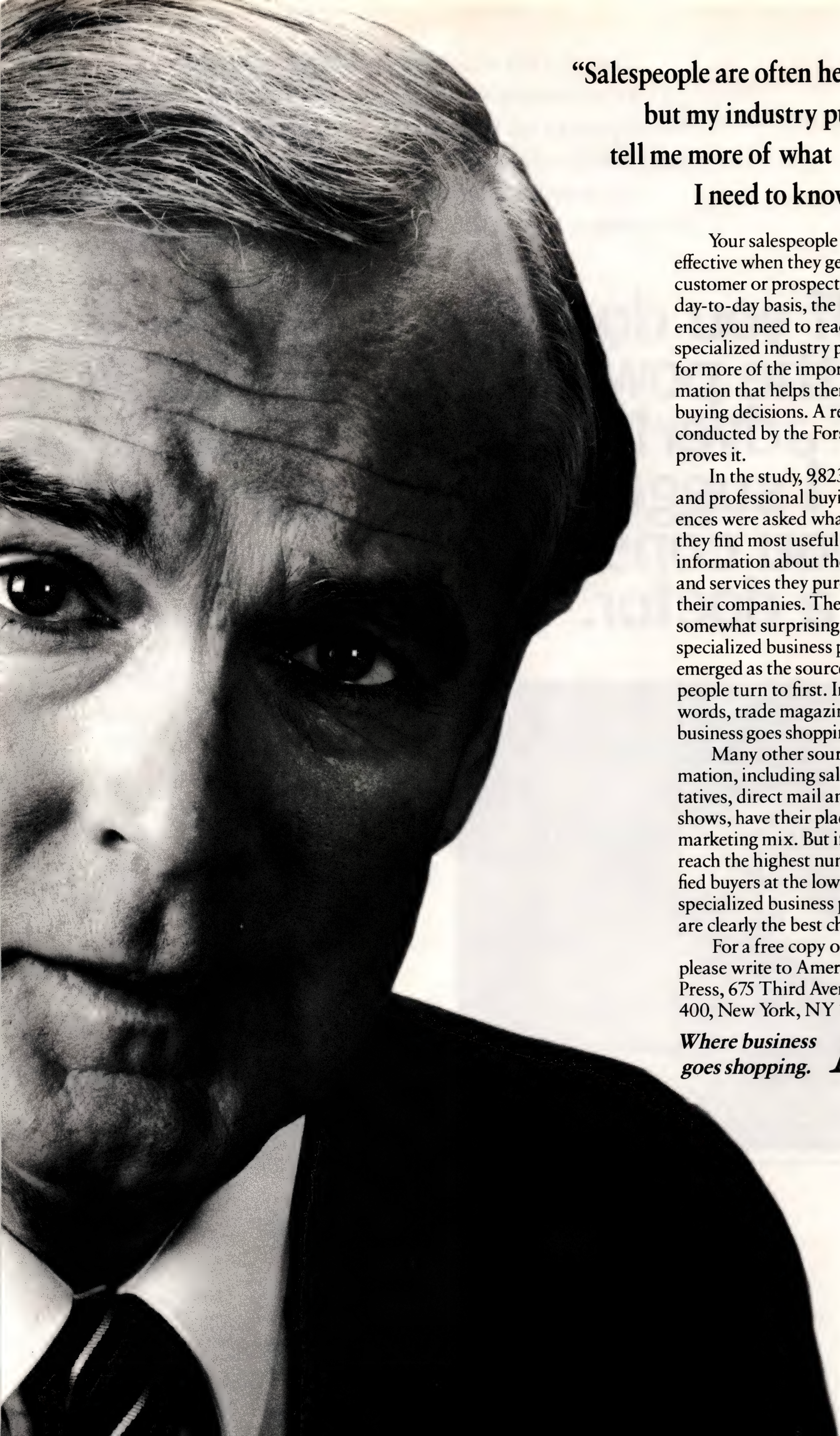
9. MULTIPLE PROCESSORS can compute the matrix of Euclidean distances an order-of-magnitude faster than a single-processor system can. This is done by first loading the feature vectors for one of the time series on successive processors. Then, the system sequentially broadcasts the feature vectors from the other time series, and concurrently computes an entire row of Euclidean distances as each feature vector is broadcast. Similarly, in determining the ideal warping path, each row of accumulated Euclidean distances is computed concurrently.

The sequence of operations to transform the time series into the frequency series includes: applying a Hanning window to the time series, performing the Fourier transform on the Hanning-weighted time series, squaring the resulting real and imaginary components, combining the adjacent real and imaginary pairs to compute the power spectrum, and finally converting the power values to decibels *(Fig. 12)*. Mapping this sequence of signal-processing computations to a multiprocessor can be accomplished simply and easily *(Fig. 13)*.

Because the original matrix-vector multiplication formulation will be used to compute the Fourier transform, the rows of the matrix are available to be pre-biased by the Hanning weighting. This effectively eliminates one of the computations. Now, consistent with the method for performing frequency analysis, one row of the Hanning-weighted cosine-sine matrix (HCS[i,j]) is loaded onto a



10. THE MOST COMMON FORM of classification is multi-template matching. Each of the templates is defined by a feature vector in M-dimensional space. The identity of an unknown feature vector to be classified is defined to be the closest match in the M-dimensional space, as determined by the minimum Euclidean distance.



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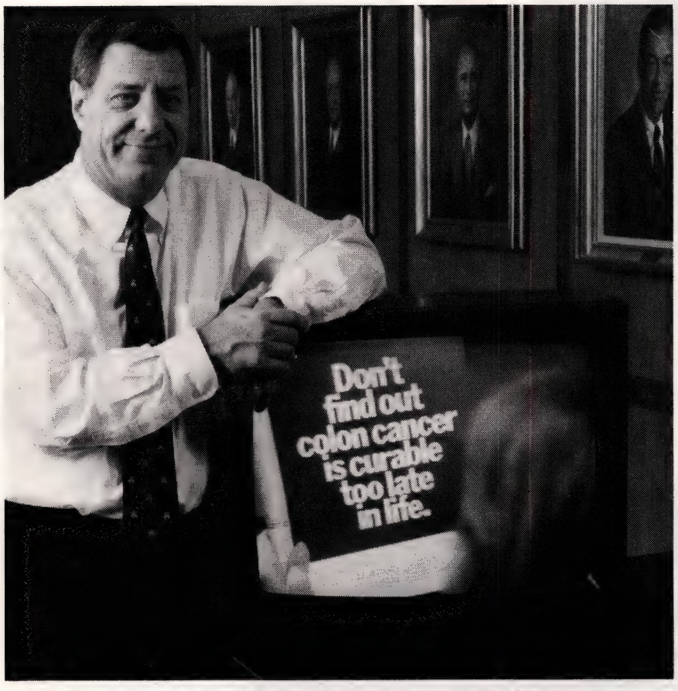
Don't find out colon cancer is curable too late in life.

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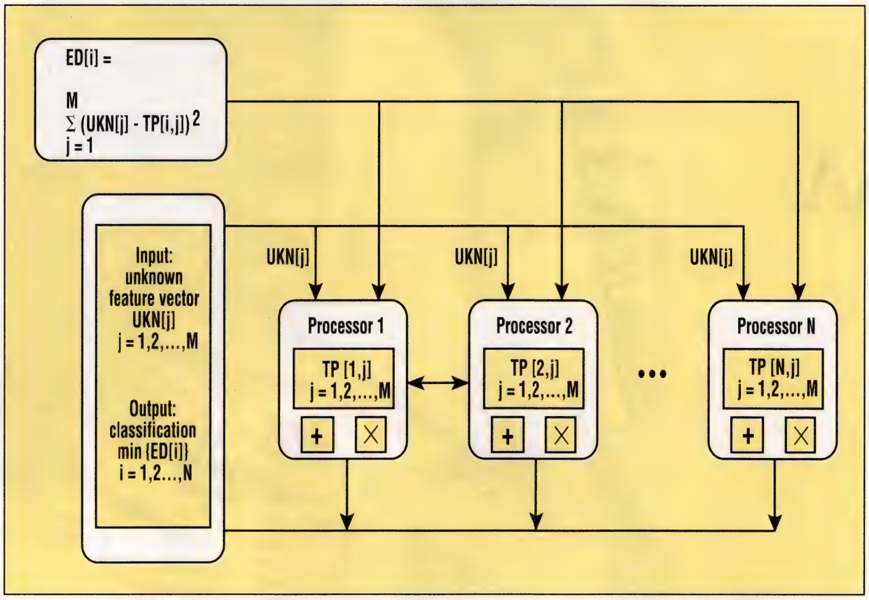

11. A MULTIPROCESSOR is ideal for performing the multi-template matching type of classification. The classification of an unknown feature vector corresponds to the processor having the minimum Euclidean distance.

separate processor. The time series is then broadcast to all of the processors. This results in the computation of the first real component on the first processor, and the first imaginary component on the second processor. The system continues to alternate real and imaginary pairs out to the Nth processor that has computed the Nth/2 imaginary component.

The next operation in the sequence is to compute the power series. First, each processor squares its real or imaginary value, so that the first processor now contains the first real component squared, the second processor contains the first imaginary component squared, and so forth. Next, each processor sends its value to its neighbor to the right and adds the received value to its own. Following this squaring, data transfer, and addition, the even-numbered processors now have the values of the power spectrum. Each processor then converts its power value to decibels using a logarithmic table lookup, and the power spectrum becomes the desired decibel frequency series. The frequency values (F[i]) can be transmitted from the even-numbered processors and collected in the shared memory. Or they may stay distributed on the processors, ready for the next computation in a yet larger sequence.

An alternative mapping of the spectral processing computations may be appropriate when computing the decibel frequency responses for a sequence of time-series snippets. In this case, it may be more efficient to load a different time-series snippet on each of the processors, and then broadcast the transfer functions. The multiprocessor speed-up realized by this mapping is immediately apparent. That's because the single-processor solution performs the computations on each time-series snippet in sequence, while the multiprocessor solution performs the computations on all of the time-series snippets at the same time (up to 512 concurrently).

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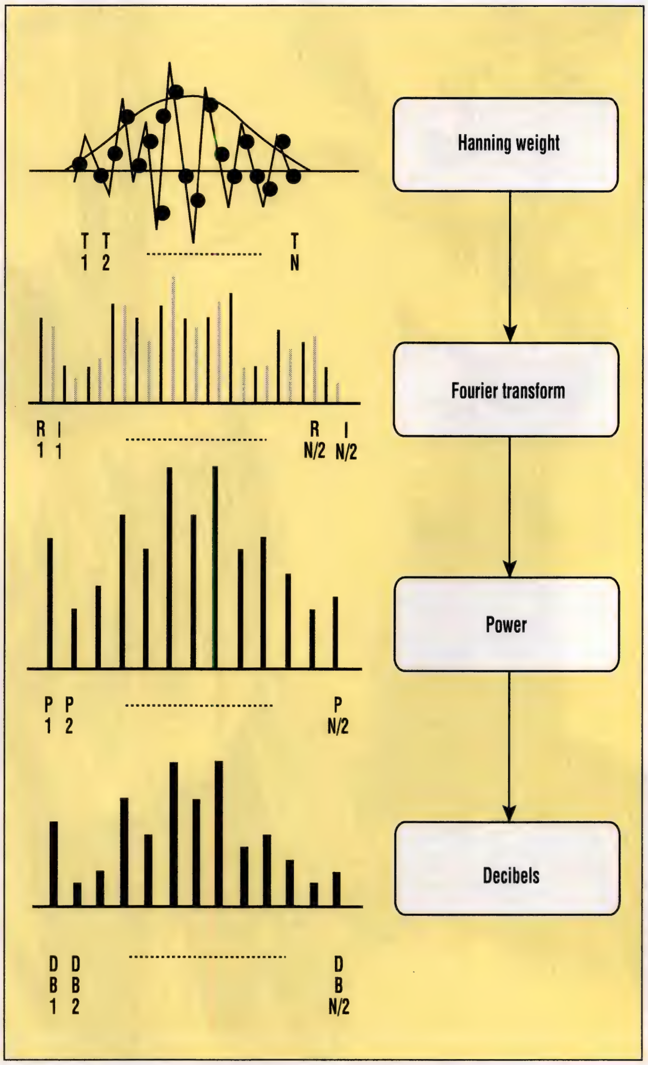

12. THE sequence of operations involved in transforming a time series into a frequency series includes: applying a Hanning window to the time series, performing the Fourier transform on the Hanning-weighted time series, squaring the resulting real and imaginary components, combining the adjacent real and imaginary pairs to compute the power spectrum, and finally converting the power values to decibels.

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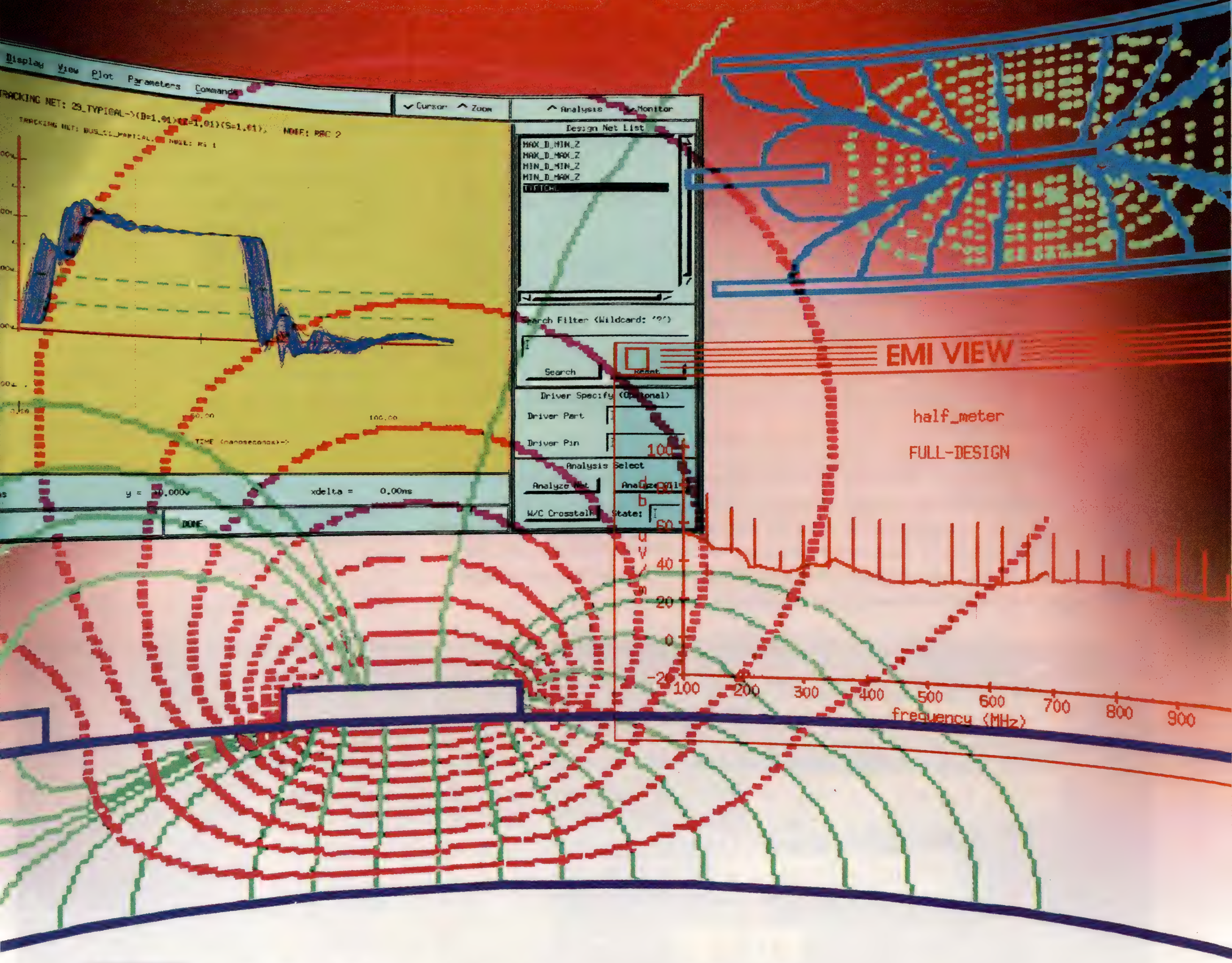

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* ***transvidiate*** *(trans vid'ē āt')* vt. ***-a ted, -a ting*** *[TRANS (L. across, over) + VID (L. videre, to see) + -IATE)]* ***1.*** *to bridge the present and future by knowing all signal distortion effects of your digital circuit design before they happen* ***2.*** *to avoid future design mistakes while the design is still a vision* ***3.*** *to exist in the future presently* ***—trans-vid'i-a'tion*** n.

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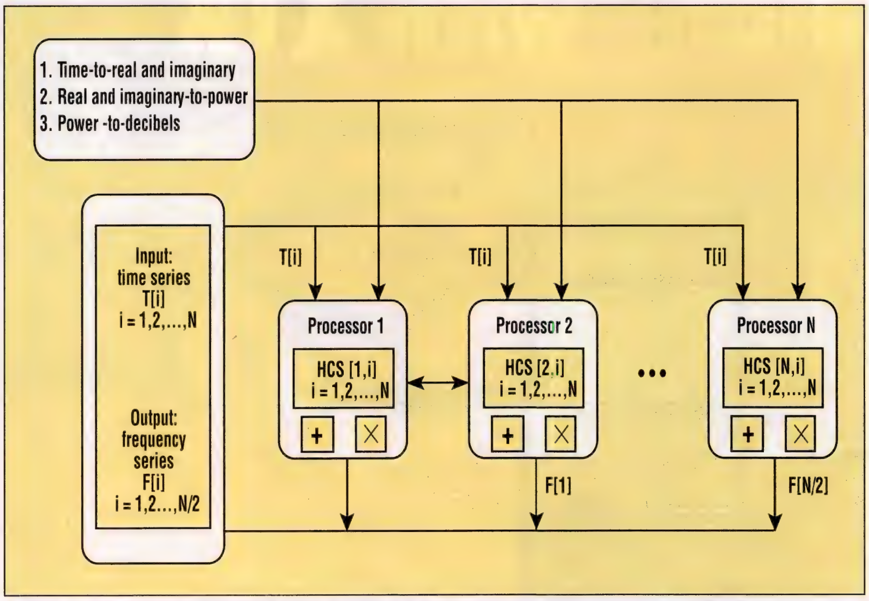

13. THREE DISTINCT OPERATIONS must take place in the multiprocessing implementation that converts a time series into a frequency series. First, the system performs a Fourier transform. The transform is determined by broadcasting the time series to the processors, which contain the rows of the Hanning-weighted cosine matrix. The resulting real and imaginary pairs are used to compute the power series, which is then computed as decibel values using a logarithmic table lookup.

lutions' CNAPS multiprocessor in real time.☐

References:
1. Cooley, J. and Tukey, J., "An Algorithm for the Machine Calculation of Complex Fourier Series," *Mathematical Computing*, April 1965.
2. Skinner, T. , Matsuura, Y., and Miyazawa, H.,"Massively Parallel DSP Technology as Applied to Speech Recognition," *DSP Applications*, August 1993.

Toby Skinner, an applications engineer at Adaptive Solutions, holds a BS in computer science from the University of Wisconsin, Madison, and an MS in speech science from the University of Minnesota, St. Paul.

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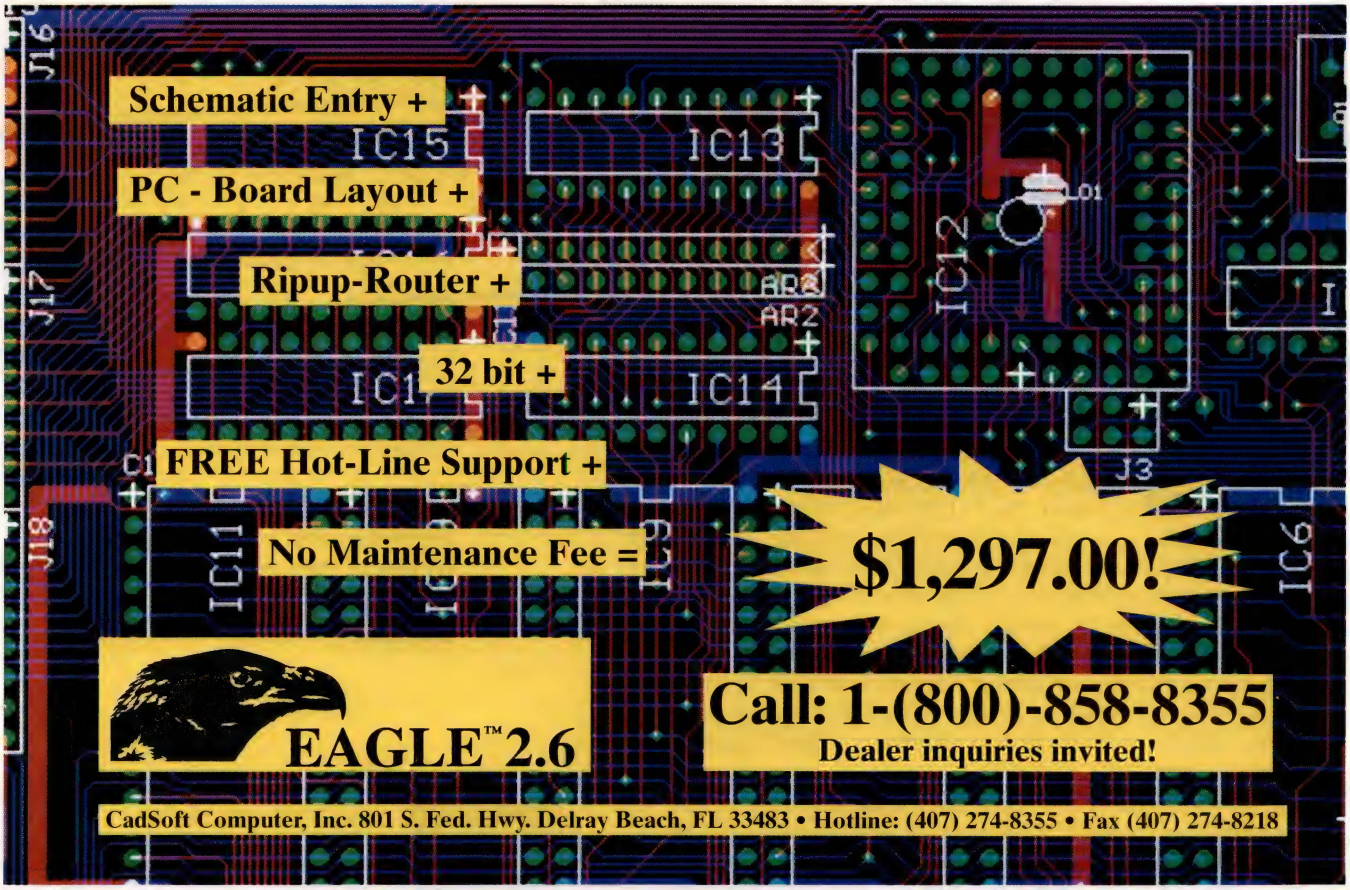
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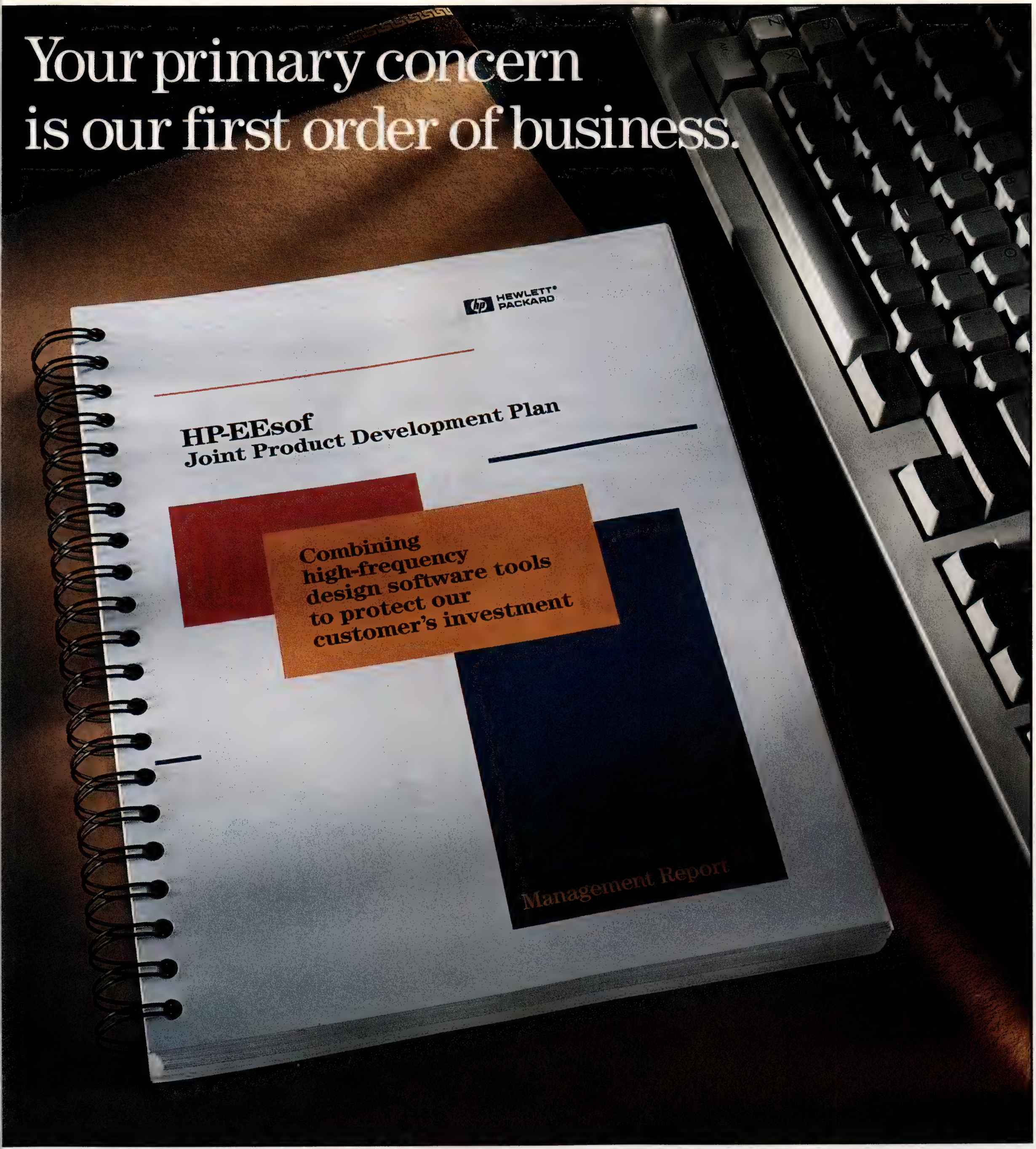
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MATCH REAL-TIME OS TO BOARDS FOR SMOOTH PORTING

AN EFFICIENT PORT TO NEW SINGLE-BOARD COMPUTERS HINGES ON HARMONIZING THE WORKINGS OF A REAL-TIME OS AND TARGET CPU.

DAVID KLANN,
STEVEN SCHULTHEIS, and DAVID SMITH
Heurikon Corp.,
8000 Excelsior Dr.,
Madison, WI 53717;
(608) 831-5500.

Ideally, a designer could rely on one procedure to port any real-time operating system to a single-board computer. Unfortunately, the architectures of the target OS and boards require that the designer customize the sequence of porting steps, particularly in deciding how the OS kernel is initially loaded into memory. Experience is needed to create the initial boot and add features and drivers to the OS image in memory without wasting time.

To simplify your efforts in porting real-time operating systems to new CPU boards, let's examine the porting process for a 68040-based single-board VMEbus computer, the HK68/V4D from Heurikon Corp. and two real-time operating systems: OS-9 developed by Microware Systems Corp., Des Moines, Iowa, and VxWorks from Wind River Systems, Alameda, Calif.

Before starting to port, remember that the target hardware may not be perfect, even if it has been tested. Basically, with new CPU boards, test software and procedures rarely exercise all of the hardware features, yet a real-time OS might. For example, tests of such features as serial ports, Small Computer Systems Interface (SCSI) ports, and Ethernet interfaces typically use simple polled I/O operations and often data loopback modes. As a result, the test code won't find bugs that arise when you transition to interrupt-driven I/O and connect with real devices.

You may also encounter bugs even if a board has been tested and another real-time OS runs on the board. Because real-time OSs vary substantially in how they handle core features like clock-tick drivers and interrupt control, a hardware design that works with one OS may cause problems with others. Furthermore, one OS may utilize more of a board's features than another—for example, some OSs don't use parity for memory and therefore wouldn't reveal bugs in the parity hardware.

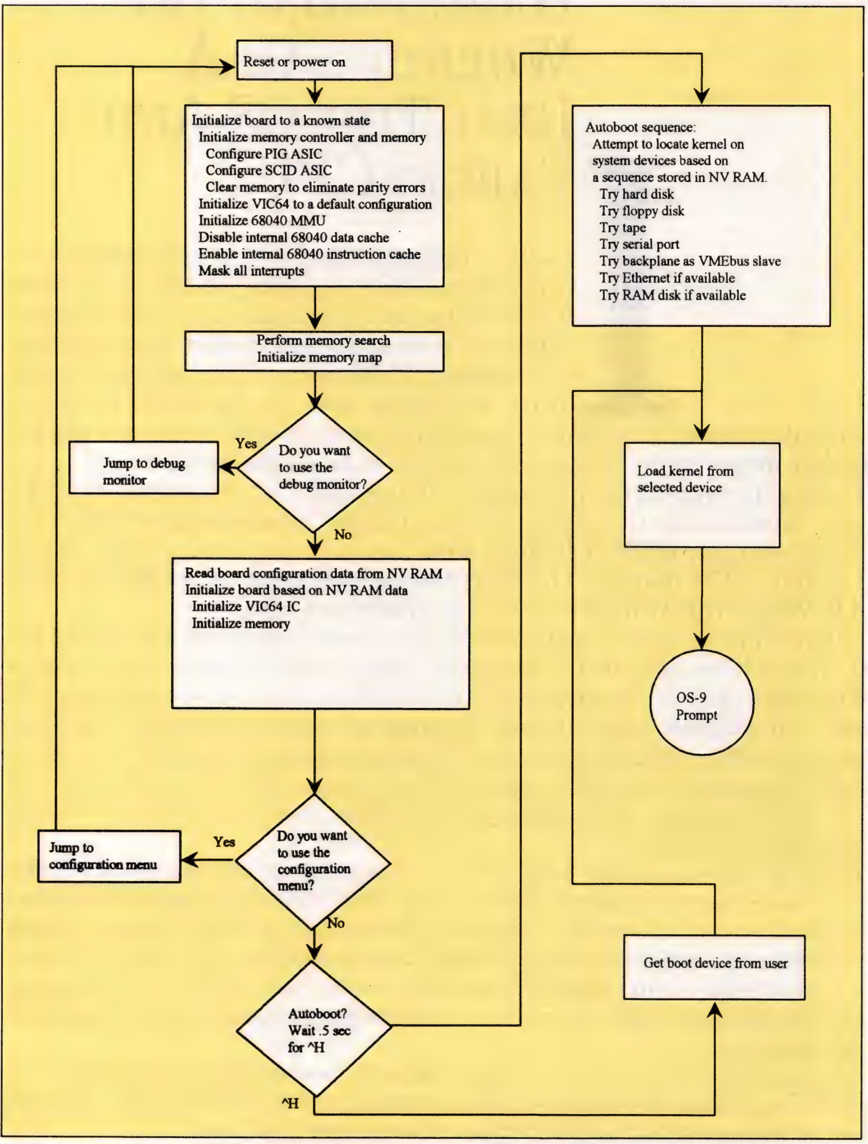
Forewarned of bugs, you can begin the process of evaluating the target OS and CPU board and developing a porting strategy. To port efficiently, planning is just as important as the code development undertaken later.

Operating-system vendors typically sell their software in a porting package that is specific to a microprocessor. This discussion assumes that you can buy the operating system in this form. Note that porting projects that start with source code and include porting the code to a new microprocessor are well beyond the scope of this discussion.

Note also that porting an OS to a target CPU board and deploying the CPU and OS with code for a specific application is a two-stage process. You first port the OS to the target CPU. Then the target is used as a development host or along with a cross-development host to develop the application for deployment.

Try to buy a porting package and options that match your hardware closely. For example, many vendors offer board support packages that include all of the code comprising a port to a specific reference design. The vendors may also offer sample drivers developed for specific peripheral ICs. Purchasing sample drivers that match your target hardware saves substantial time.

As a first step, make a table comparing features of the target hardware with the features of the target operating system and the resources offered in port packages, board support packages, and optional drivers. With such a table, you can quickly compare the minimal hardware features required to run an OS (typically listed in the porting documentation) with the target hardware features and the OS features. Such a comparison helps quantify the scope of the porting effort. Most important, it's the basis for laying out the sequence of steps to port the OS.


Reset or power on
Initialize board to a known state
Initialize memory controller and memory
Configure PIG ASIC
Configure SCID ASIC
Clear memory to eliminate parity errors
Initialize VIC64 to a default configuration
Initialize 68040 MMU
Disable internal 68040 data cache
Enable internal 68040 instruction cache
Mask all interrupts
Perform memory search
Initialize memory map
Do you want to use the debug monitor?
Yes
Jump to debug monitor
No
Read board configuration data from NV RAM
Initialize board based on NV RAM data
Initialize VIC64 IC
Initialize memory
Do you want to use the configuration menu?
Yes
Jump to configuration menu
No
Autoboot? Wait .5 sec for ^H
^H
Autoboot sequence:
Attempt to locate kernel on system devices based on a sequence stored in NV RAM.
Try hard disk
Try floppy disk
Try tape
Try serial port
Try backplane as VMEbus slave
Try Ethernet if available
Try RAM disk if available
Load kernel from selected device
OS-9 Prompt
Get boot device from user

1. A FLOW DIAGRAM helps designers clarify the target OS architecture and requirements for new code by considering the sequence of events in booting for the target OS. In this case, the OS-9 real-time operating system created by Microware Systems Corp. is the target OS.

To determine the best sequence for porting an OS, you must consider four key parameters:

- CPU-board hardware implementation
- Binary and source modules offered by the OS vendor
- Architecture of the real-time OS
- Requirements of the target application

A hardware/software comparison table gives a snapshot of the hardware features and OS features that can be related to a target application. For example, a general-purpose CPU board may have on-board Ethernet support as a standard or optional feature. Your application may require Ethernet or another LAN. And the target OS may or may not include Ethernet support as a standard feature. Moreover, the OS architecture may rely heavily on a LAN for development or may simply offer LAN support as an I/O option.

For instance, OS-9 doesn't include network support as a standard feature but Microware does offer optional Ethernet (transmission control protocol/Internet protocol, or TCP/IP) support, including a sample driver for several chips, such as the 82596CA Ethernet IC. Therefore, including Ethernet support in an OS-9 port to a board that uses the 82596CA IC would take little time.

LAN support, though, isn't required in many OS-9 applications. OS-9 can be strictly ROM resident, and it can be booted from various I/O devices that include LANs and, more typically, disk or tape drives. Therefore, even if your target application requires Ethernet support, development and porting of the Ethernet driver shouldn't be an early priority in the overall porting process.

Conversely, the typical VxWorks software-development environment is LAN-based with a cross-development host, such as a Sun workstation. You can use OS-9 in a similar manner, but the more typical configuration is a OS-9-hosted development system. Because VxWorks is designed for LAN-based development, you want to get Ethernet working early in the porting process

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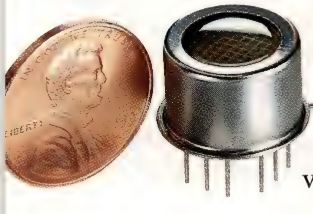

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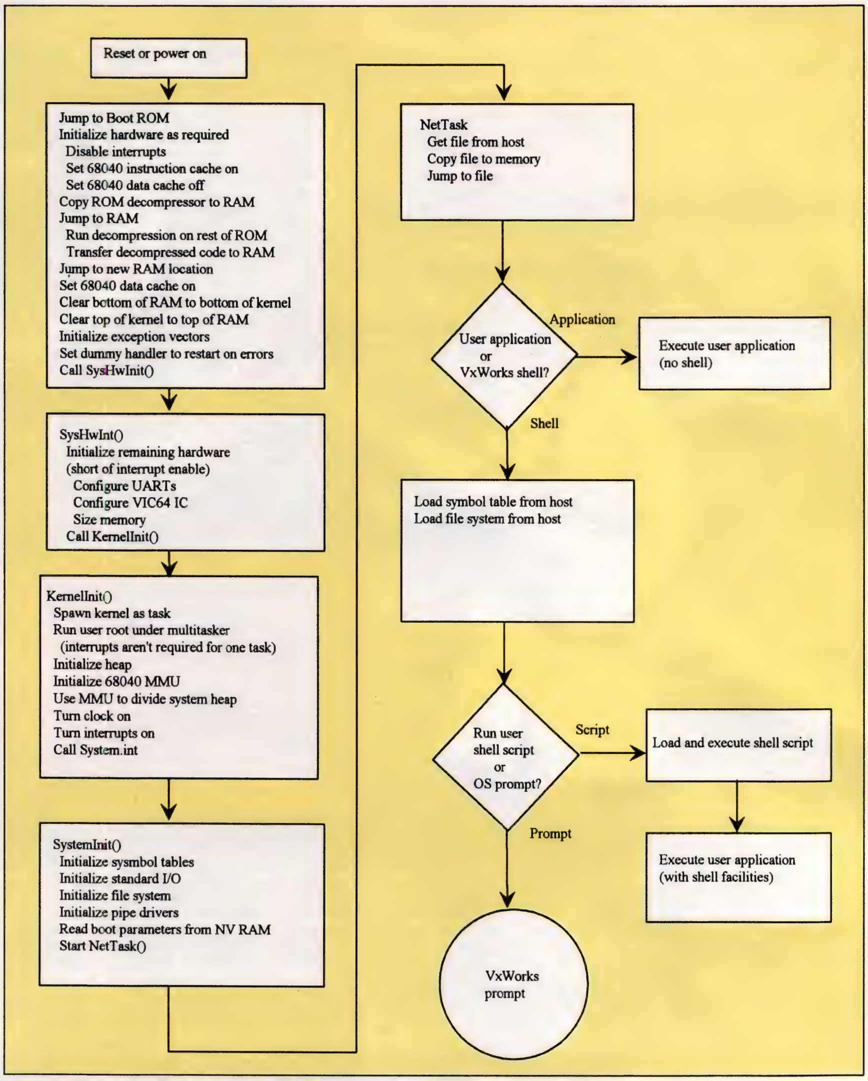
Reset or power on
Jump to Boot ROM
Initialize hardware as required
Disable interrupts
Set 68040 instruction cache on
Set 68040 data cache off
Copy ROM decompressor to RAM
Jump to RAM
Run decompression on rest of ROM
Transfer decompressed code to RAM
Jump to new RAM location
Set 68040 data cache on
Clear bottom of RAM to bottom of kernel
Clear top of kernel to top of RAM
Initialize exception vectors
Set dummy handler to restart on errors
Call SysHwInit()
SysHwInt()
Initialize remaining hardware
(short of interrupt enable)
Configure UARTs
Configure VIC64 IC
Size memory
Call KernelInit()
KernelInit()
Spawn kernel as task
Run user root under multitasker
(interrupts aren't required for one task)
Initialize heap
Initialize 68040 MMU
Use MMU to divide system heap
Turn clock on
Turn interrupts on
Call System.int
SystemInit()
Initialize sysmbol tables
Initialize standard I/O
Initialize file system
Initialize pipe drivers
Read boot parameters from NV RAM
Start NetTask()
NetTask
Get file from host
Copy file to memory
Jump to file
User application or VxWorks shell?
Application
Execute user application (no shell)
Shell
Load symbol table from host
Load file system from host
Run user shell script or OS prompt?
Script
Load and execute shell script
Execute user application (with shell facilities)
Prompt
VxWorks prompt

2. A FLOW DIAGRAM for VxWorks developed by Wind River Systems defines a typical boot sequence for the real-time OS. An important task for designers is determining what code must be developed for putting an OS image in the target CPU's memory and deciding how best to implement it.

so that cross-development and -debugging tools can be used. With VxWorks, knowledge of the OS architecture correctly leads you to work on Ethernet early in the porting process even if your end application doesn't require Ethernet. This holds true if Ethernet isn't included on your target hardware and a dedicated Ethernet board must be used in the VMEbus rack.

BOOT SEQUENCE

The target OS architecture and requirements can be clarified for new code by considering the sequence of events in booting your target OS. Flow diagrams *(Figs. 1 and 2)* define a typical boot sequence for OS-9 and VxWorks. You need to determine how to put an OS image in the target CPU's memory the first time and what code must be developed to accomplish the task.

You can count on only a couple of necessities as you plan the porting process. Usually you need a simple polled-I/O serial port routine that provides a link to a local terminal. Also required is an on-board monitor program that allows you to use a terminal to address memory locations from the terminal and to jump to a location and begin execution.

When considering the code that you need to develop, start with the boot ROM. That's because all systems must have such a ROM, though its size and structure may vary significantly. The boot ROM could incorporate a number of functional modules, including hardware configuration and initialization routines, parts of the OS kernel or file system, and simplified or full-scale drivers for boot devices.

For example, the OS-9 boot ROM on the V4D board includes a setup routine that operates similarly to the setup capability used on IBM-compatible personal computers. With the ROM routine, users can configure parameters like interrupt levels; choose among valid boot devices; and configure memory partitions with such parameters as cacheable or non-cacheable.

OS-9 boot ROMs also include simple drivers for all boot devices. The difference between the boot driver and the run-time driver varies from device to device and OS to OS. In general, minimizing boot-driver size is a good idea because it saves ROM space. But in many embedded applications, the ROM may be the only nonvolatile storage element on the system, thereby forcing you to include run-time drivers in ROM.

The serial driver included in an OS-9 boot ROM, for example, allows terminal operation and can even be used as a boot device. But the boot driver doesn't make use of interrupts and is much less capable and smaller than the serial driver required at run time.

Conversely, OS-9 boot drivers for SCSI disk drives and other devices should closely match the run-time driver. In fact, consider the driver development a single project and use compiler switches to distinguish the boot code from the run-time code. In porting VxWorks, you needn't distinguish between boot drivers and run-time drivers because the OS needs support for all devices in ROM, whether you're working in a development environment or deploying a system.

The code that you create for a boot ROM will likely include assembly language to initialize the hardware and C for most other functions, including drivers. OS vendors typically incorporate sample boot ROMs to which you add hardware-specific code. Although a boot ROM starts the booting process, it may neither

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Mike Quinlan, Chairman, CEO McDonald’s (left)

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be the best place to start an OS port nor the best way to initially load the OS image into memory. After considering the hardware, the application, and the target OS, you should be able to develop a flow diagram for the porting process similar to the diagrams for OS-9 *(Fig. 3)* and VxWorks *(Fig. 4)*.

As Fig. 4 shows, creating a boot ROM is one of the last required steps in porting VxWorks. VxWorks is more easily ported by using a board that already runs VxWorks in the same VMEbus rack as the target CPU. The operational CPU, with onboard Ethernet or used with a VMEbus Ethernet board, can download code into memory on the new target. The new target requires only a monitor that can map memory and jump to an address and begin execution.

VERIFYING HARDWARE

The early steps of the VxWorks porting process help verify basic operation of the hardware—ensuring that the target CPU can read and write local memory as well as VMEbus memory. If bugs occur in this phase, fix them with debugging tools (VMEbus analyzers, ROM emulators, etc.) and continue.

This recommended sequence of steps is optimal for VxWorks ports for two reasons. First, VxWorks modifies processor resources, such as status registers and trap vectors, on startup. Therefore, the VxWorks ROM-based debugging monitor can get confused when you use it to set breakpoints or perform trace operations. Using a second operational CPU offers primitive access to VxWorks debugging tools to examine memory on the target and perform the iterative steps necessary to get the target working. Early on in debugging, the developer needs to make liberal use of "printif" statements to memory so that the working CPU can trace the operation of the new target.

Second, VxWorks requires a cross-development host that communicates with the target CPU through TCP/IP protocols—typically over Ethernet. The sequence of porting steps proposed here (including working on Ethernet support early on) makes the full VxWorks debugging environment available on the target CPU as early as possible in the overall process. While the sequence doesn't enable you to directly boot the target via Ethernet, the two-board scheme can be used to download a new OS image and run debugging sessions through Ethernet.

While you could port OS-9 in a similar manner as VxWorks, the port will likely be faster following the steps outlined in Fig. 3. Because OS-9 is a disk-based software-development host in its native mode, developing a boot ROM and loading an OS image from disk or tape is a priority in most OS-9 ports.

As a result, a recommended OS-9 port process, therefore, starts with a tried-and-true development process—develop some code, burn an EPROM, test and debug the code in the EPROM, add more features to the code, and burn another EPROM. Experienced programmers can use this EPROM-based approach to test large segments of the boot code quickly.

OS-9 does offer alternatives for less experienced software developers. The OS allows the developer to first bring up a simple kernel via EPROMs and then incrementally add, debug, and test code that is downloaded via a serial port.

In OS-9 ports (and VxWorks ports for that matter), the sequence of events outlined in Fig. 3 include intermediate steps in reaching the goal of an initial boot. In fact, the simplest way of getting an OS-9 kernel image into memory is to boot from ROM—essentially executing a kernel that resides in ROM. The initial kernel won't have much support for the target hardware included but will allow you limited access to the debugger included in the kernel.

Regardless of how you attempt to first place an image of any OS in memory, early on you must develop code for hardware initialization. As a result, your progress depends upon specific hardware details, such as the type of clock and interrupt controller on the board and the board's memory architecture. As in the OS-9 boot sequence in Fig. 1, the ROM must immediately perform hardware initialization.

In fact, a functional unit as simple as a clock IC can slow your software-development progress as you address it for the first time. For instance, consider the TIC (Time In a Can) developed by Dallas Semiconductor, Texas. The TIC contains a battery, 512 bytes of nonvolatile RAM (NVRAM), and a real-time clock/calendar.

The compact TIC device employs a serial-like interface for access to the RAM and the clock. The V4D board interfaces the 68040 processor to the TIC through a serial connection handled by two ASICs—the PIG (Peripheral Interface Gate) array) and SCID (serial connector interface device). They control the memory subsystem and provide timer facilities and UARTs for the CPU board.

The only disadvantage to the TIC and the V4D implementation is that the serial interface results in relatively slow access to the clock and configuration memory; as a result, several seconds are required for writes that update all 512 bytes of memory in the TIC. The slow access typically isn't a problem, though, because systems read the TIC only after a reset or upon power-up and write to the TIC only during rare system configurations.

SERIAL RAM ACCESS

However, the TIC may add other difficulties to the early stages of an OS-9 port because of the way in which data must be read and written to the device. The TIC calls for a series of accurately timed pulses on a control line for RAM or clock access. So the code to initialize the V4D hardware must generate the correct timing sequence for access. But OS-9 boot sequences typically execute directly out of ROM or EPROM. And ROM access speeds are low enough to keep the 68040 processor from accessing instructions quickly enough to generate the timing sequence necessary to access the TIC.

The ultimate solution, though simple, isn't necessarily consistent with typical OS-9 boot sequences. The boot-ROM code enables the 68040 instruction cache and then makes a dummy access to EPROM, thereby copying key timing routines from EPROM into the cache. Executing out of cache, the processor can perform the timed access to the serial NVRAM and clock correctly. Typically, however, the OS-9 boot ROM won't enable the cache because decisions on the use of the data and instruction caches are left to the application programmer.

Moreover, enabling the cache requires that the hardware initialization code in the ROM perform additional memory-management functions to prevent errors from sources like parity-checking hardware. Despite these facts, enabling the cache causes no real problems because application programs can still manipulate the cache configuration after boot.

The TIC implementation on the V4D is a good example of how a simple hardware feature can affect different operating systems in completely different ways. For instance, VxWorks in a typical configuration begins life by copying its ROM code into RAM. And executing out of RAM, the TIC initialization routines work fine with or without the instruction cache enabled.

SIMPLIFY DEVELOPMENT

After loading the kernel, you can use the kernel tools to develop and debug a serial-port driver. In most cases, the code that controls serial communications with a local terminal during the early stages of the port is part of a ROM monitor on the target CPU board. What's more, the monitor uses polled I/O operations and doesn't resemble an OS serial-port driver in any way.

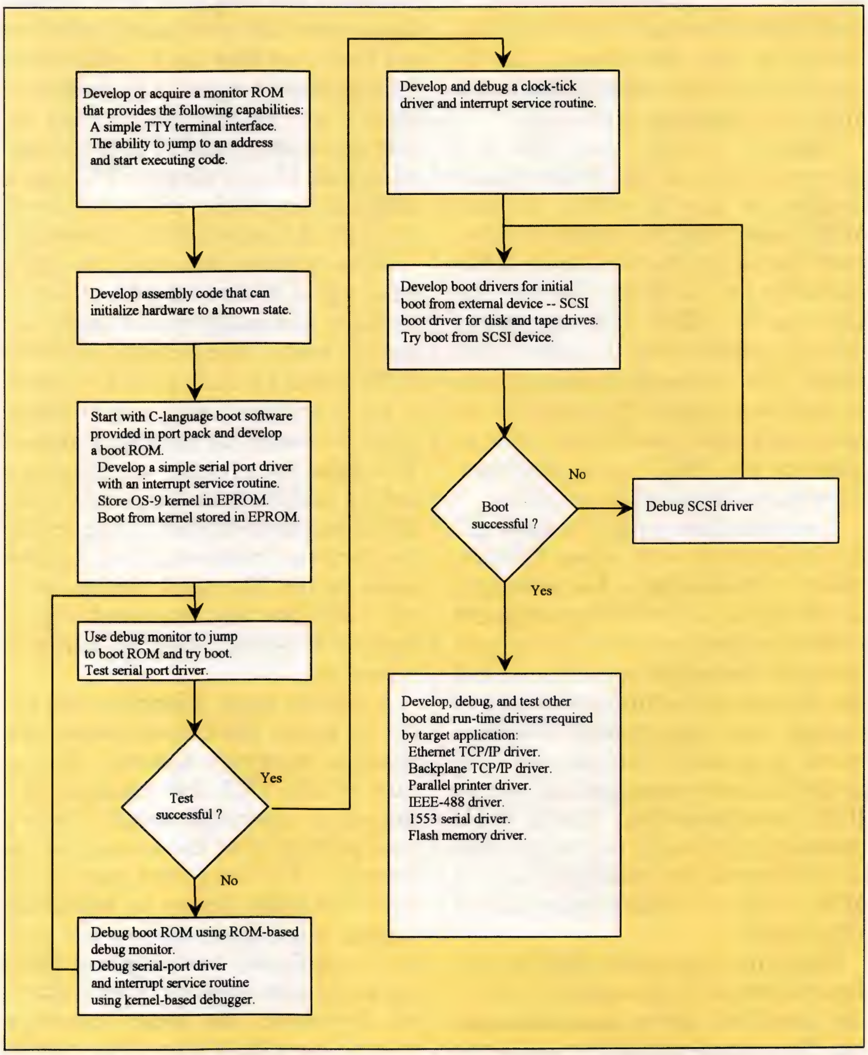
To continue the OS port, you need to develop a serial-port driver that supports circular transmitting and receiving buffers, multiple baud rates, and interrupt-driven operation. The serial-port driver is likely to be the first test of how the OS port handles interrupts. The driver code includes an interrupt service routine (ISR) that can respond to a kernel query to see if a serial port caused an interrupt. When a serial port causes the interrupt, the service routine must also handle the interrupt, such as by moving a character from a receive buffer. The driver must also include the hooks that application programs use to access serial ports.

Serial-port drivers are good examples of how the architectures of two real-time OSs can differ. VxWorks breaks the serial-port driver into two sections. The porting package includes binary code for a generic block driver for serial devices. The binary driver contains the code that implements buffers, moves data, and makes calls to a set of device-dependent routines that address the UART on the target CPU. You port a driver by developing the routines that can address the UART, set parameters such as baud rate and parity, and read or write data. Of course, you get samples of these device specific routines.

OS-9, in contrast, implements the serial driver in a single code module and provides samples of serial-driver source code for specific UARTs. The code required for either scenario is similar—in either case, you must add the device-specific routines. You may find debugging simpler, however, with the entire source module.

TRAFFIC JAM

When you start debugging a serial-port driver, there's the immediate obstacle of debugging code designed to perform with the serial hardware that's used to simultaneously access the kernel and debugger. Fortunately, most CPU boards and UART ICs include more than one serial port. You can configure the serial driver to use one or more ports that aren't required for terminal activity and debug the driver. Later, adding support for the terminal port, at most, exposes the risk of using the wrong


Develop or acquire a monitor ROM that provides the following capabilities:
A simple TTY terminal interface.
The ability to jump to an address and start executing code.
Develop assembly code that can initialize hardware to a known state.
Start with C-language boot software provided in port pack and develop a boot ROM.
Develop a simple serial port driver with an interrupt service routine.
Store OS-9 kernel in EPROM.
Boot from kernel stored in EPROM.
Use debug monitor to jump to boot ROM and try boot.
Test serial port driver.
Test successful ?
Yes
No
Debug boot ROM using ROM-based debug monitor.
Debug serial-port driver and interrupt service routine using kernel-based debugger.
Develop and debug a clock-tick driver and interrupt service routine.
Develop boot drivers for initial boot from external device -- SCSI boot driver for disk and tape drives.
Try boot from SCSI device.
Boot successful ?
No
Debug SCSI driver
Yes
Develop, debug, and test other boot and run-time drivers required by target application:
Ethernet TCP/IP driver.
Backplane TCP/IP driver.
Parallel printer driver.
IEEE-488 driver.
1553 serial driver.
Flash memory driver.

3. IN ITS NATIVE MODE **OS-9 is a disk-based software development host. As a result, developing a boot ROM and loading an OS image from disk or tape is a priority in most OS-9 ports.**

address to access the UART, which requires a simple fix.

If you have to port a driver to a CPU with a single UART, there are two ways to go. First, you can add a second UART via a second board or a mezzanine card, even if your end application doesn't require a second UART. Second, you can use a tool like a ROM emulator to debug the code and then make the step of transitioning terminal I/O to the serial-port driver.

The next steps, some of the most difficult in porting, involve starting the multitasking operation—the serial-port driver that's tested first executes as the only task on the system. To invoke tasking, if your target OS and CPU support a memory-management unit (MMU), make sure it's operating. Then port and test a clock-tick driver and start the multitasker so that the system can be transitioned into normal interrupt-driven multitasking operation.

Ports of VxWorks and OS-9 to a processor such as the 68040 usually require no special effort to port MMU code. First, the kernels include code that supports the on-chip MMU explicitly on the 68040. Second, the OSs use the MMU only to protect memory regions and to assign attributes like cacheable/noncacheable to specific regions. Thus the OSs require only that you develop code to initialize the MMU during the hardware initialization phase of a boot.

You could face a slightly more difficult situation with other OS/processor combinations. For example, an OS such as LynxOS that supports virtual memory requires you to port the code that pages segments in and out of memory before proceeding to engage the multitasker. Furthermore, processors lacking an integrated memory-management unit or RISC processors that handle MMU routines in software may require the development or modification of MMU code to match your target CPU board.

Once you're sure the MMU is configured properly, you can proceed to the clock-tick driver and multitasking. The complexity of the clock-tick driver varies according to your OS and the target hardware. In general, the clock driver provides the time-slice interrupt to the kernel as the basis for multitasking and supplies the facility for the OS or application software to read or write a real-time clock.

STARTING A TIMER

The first task of the clock driver is to configure and start a timer. On the V4D, for example, the PIG ASIC includes timers that can divide a clock to achieve the desired interrupt interval for multitasking. The driver must initialize the timer so that it interrupts the CPU on a regular basis. For example, the OS-9 clock driver for the V4D sets the timer to interrupt the CPU every 10 ms.

Like the serial driver, the clock driver includes an ISR that can verify whether clock circuitry caused an interrupt and responds with service if necessary. In some cases, your target hardware may use a dedicated interrupt level to signal a time-slice interrupt (or, for that matter, any interrupt source could have a dedicated signal). If your target CPU uses a dedicated level, the ISR won't need to verify the source of the interrupt.

In many cases, however, the clock interrupt is combined with other interrupts and mapped to a single interrupt vector. For example, the PIG ASIC on the V4D integrates two serial ports and the timer, and all three facilities share an interrupt signal. You have to provide an interrupt polling table in your port to allow the OS to handle interrupts from multiple hardware resources that use the same vector. You must create a polling table for any interrupt signal that could be triggered by multiple resources.

A polling table prioritizes the order in which the kernel checks the possible interrupt sources. In the case of the V4D, for example, the time-slice interrupt would always take priority over the serial-port interrupts. The time-slice portion of your clock-tick driver is relatively simple. Most timer devices are simple to configure, and they run without assistance once the timer is started. Moreover, the timer interrupt routine does little more than verify the source of the interrupt, thereby enabling the kernel multitasker module to swap tasks.

The second part of the clock-tick driver—reading and writing time and date from a clock chip—can actually be more complicated. In the driver, first you have to develop the code that can access the hardware correctly. Then you must provide the code to convert the formats of the clock data used in the OS and the clock chip.

DATE TRANSLATION

Neither clock formats in OS drivers nor clock chips are as simple as registers holding ASCII digits that represent each part of the time or date. Clock chips and OS kernel clock routines typically use a reference date and an offset, from which the exact time and date can be calculated. For example, OS-9's kernel uses a reference date of Jan. 1, 4173 BC based on the Julian calendar. Therefore, the OS requires an offset measured in Julian days and remainder seconds to calculate the present date. Storing the offset requires a 32-bit slot for the Julian day offset and a 32-bit slot for the remainder seconds. The clock device on your target CPU could do things quite differently. For example, the TIC device on the V4D allows users to define a reference date and store an offset to that date in seconds.

With the OS-9 and TIC combination, you can't simply set the TIC reference date to 4173 BC (the OS-9 reference date) because the TIC offset stored in seconds isn't large enough to measure time in the 20th century. Therefore, you have to establish an alternate reference date such as Jan. 1, 1900. For OS-9 to read the TIC, your clock routine must convert the TIC offset time (measured in seconds) to Julian days and seconds and then add the number of Julian days and seconds that elapsed between 4173 BC and Jan. 1, 1900. There's also another gotcha to beware of: Some OSs and clock devices measure an offset from the previous midnight to keep time; others measure an offset until the next midnight to keep time.

While time conversion causes a logic problem, actually reading and writing the clock device can create other difficulties. Most likely, you have already developed the low-level routines necessary to access the

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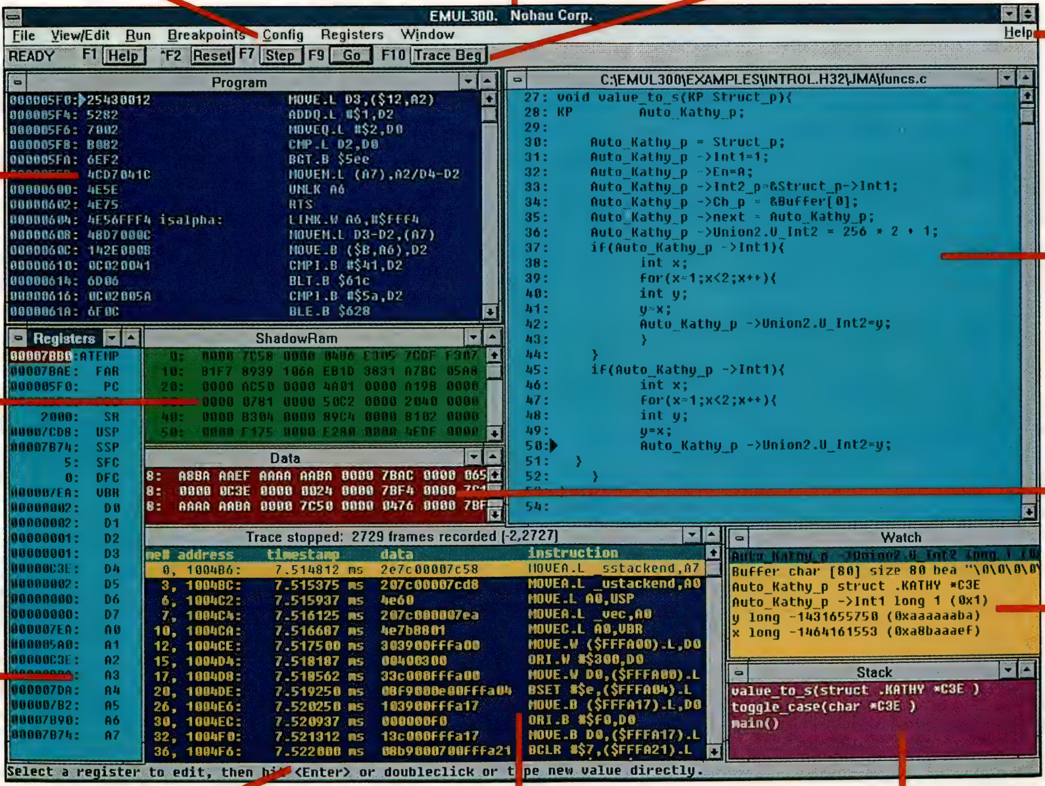

```
000005F0:25430012                    MOVE.L D3,($12,A2)
000005F4: 5282                       ADDQ.L #$1,D2
000005F6: 7002                       MOVEQ.L #$2,D0
000005F8: B082                       CMP.L D2,D0
000005FA: 6EF2                       BGT.B $5ee
          4CD7041C                   MOVEM.L (A7),A2/D4-D2
00000600: 4E5E                       UNLK A6
00000602: 4E75                       RTS
00000604: 4E56FFF4 isalpha:          LINK.W A6,#$FFF4
00000608: 48D7000C                   MOVEM.L D3-D2,(A7)
0000060C: 142E000B                   MOVE.B ($B,A6),D2
00000610: 0C020041                   CMPI.B #$41,D2
00000614: 6D06                       BLT.B $61c
00000616: 0C02005A                   CMPI.B #$5a,D2
0000061A: 6F0C                       BLE.B $628
```

```
000078B0:ATEMP
000078AE:   FAR
000005F0:    PC

    2000:    SR
00007CD8:   USP
00007B74:   SSP
       5:   SFC
       0:   DFC
000007EA:   VBR
00000002:    D0
00000002:    D1
00000001:    D2
00000001:    D3
00000C3E:    D4
00000002:    D5
00000000:    D6
00000000:    D7
000007EA:    A0
000005A0:    A1
00000C3E:    A2
         :   A3
000007DA:    A4
000007B2:    A5
00007B90:    A6
00007B74:    A7
```

```
 0:  0000 7C58 0000 0406 E305 7CDF F307
10:  81F7 8939 106A EB1D 3831 A78C 05A8
20:  0000 AC50 0000 4A01 0000 A198 0000
     0000 0781 0000 50C2 0000 2040 0000
40:  0000 B304 0000 89C4 0000 8102 0000
50:  0000 F175 0000 E2AA 0000 4FDF 0000
```

```
8:  ABBA AAEF AAAA AABA 0000 7BAC 0000 065
8:  0000 0C3E 0000 0024 0000 7BF4 0000
8:  AAAA AABA 0000 7C50 0000 0476 0000 78F
```

```
void value_to_s(KP Struct_p){
KP          Auto_Kathy_p;

    Auto_Kathy_p = Struct_p;
    Auto_Kathy_p ->Int1=1;
    Auto_Kathy_p ->En=A;
    Auto_Kathy_p ->Int2_p=&Struct_p->Int1;
    Auto_Kathy_p ->Ch_p = &Buffer[0];
    Auto_Kathy_p ->next = Auto_Kathy_p;
    Auto_Kathy_p ->Union2.U_Int2 = 256 * 2 + 1;
    if(Auto_Kathy_p ->Int1){
          int x;
          for(x=1;x<2;x++){
          int y;
          y=x;
          Auto_Kathy_p ->Union2.U_Int2=y;
          }
    }
    if(Auto_Kathy_p ->Int1){
          int x;
          for(x=1;x<2;x++){
          int y;
          y=x;
          Auto_Kathy_p ->Union2.U_Int2=y;
  }
    }

```

```
Trace stopped:  2729 frames recorded [-2,2727]
me# address   timestamp    data                 instruction
  0, 1004B6:  7.514812 ms  2e7c00007c58         MOVEA.L  sstackend,A7
  3, 1004BC:  7.515375 ms  207c00007cd8         MOVEA.L _ustackend,A0
  6, 1004C2:  7.515937 ms  4e60                 MOVE.L A0,USP
  7, 1004C4:  7.516125 ms  207c000007ea         MOVEA.L _vec,A0
 10, 1004CA:  7.516687 ms  4e7b8801             MOVEC.L A0,VBR
 12, 1004CE:  7.517500 ms  303900FFFa00         MOVE.W ($FFFA00).L,D0
 15, 1004D4:  7.518187 ms  00400300             ORI.W #$300,D0
 17, 1004D8:  7.518562 ms  33c000FFFa00         MOVE.W D0,($FFFA00).L
 20, 1004DE:  7.519250 ms  08F9000e00FFFa04     BSET #$e,($FFFA04).L
 26, 1004E6:  7.520250 ms  103900FFFa17         MOVE.B ($FFFA17).L,D0
 30, 1004EC:  7.520937 ms  000000F0             ORI.B #$F0,D0
 32, 1004F0:  7.521312 ms  13c000FFFa17         MOVE.B D0,($FFFA17).L
 36, 1004F6:  7.522000 ms  08b9000700FFFa21     BCLR #$7,($FFFA21).L
```

```
Auto_Kathy_p ->Union2.U_Int2 long 1 (0x
Buffer char [80] size 80 bea "\0\0\0\0
Auto_Kathy_p struct .KATHY *C3E
Auto_Kathy_p ->Int1 long 1 (0x1)
y long -1431655750 (0xaaaaaaba)
x long -1464161553 (0xa8baaaef)
```

```
value_to_s(struct .KATHY *C3E )
toggle_case(char *C3E )
main()
```

```
Select a register to edit, then hit <Enter> or doubleclick or type new value directly.
```

isassembler,
in-line
assembler
Window

hadow RAM
shows data
anges in real-
ne. This data
can be trans-
rted to other
Windows
programs
hrough DDE.

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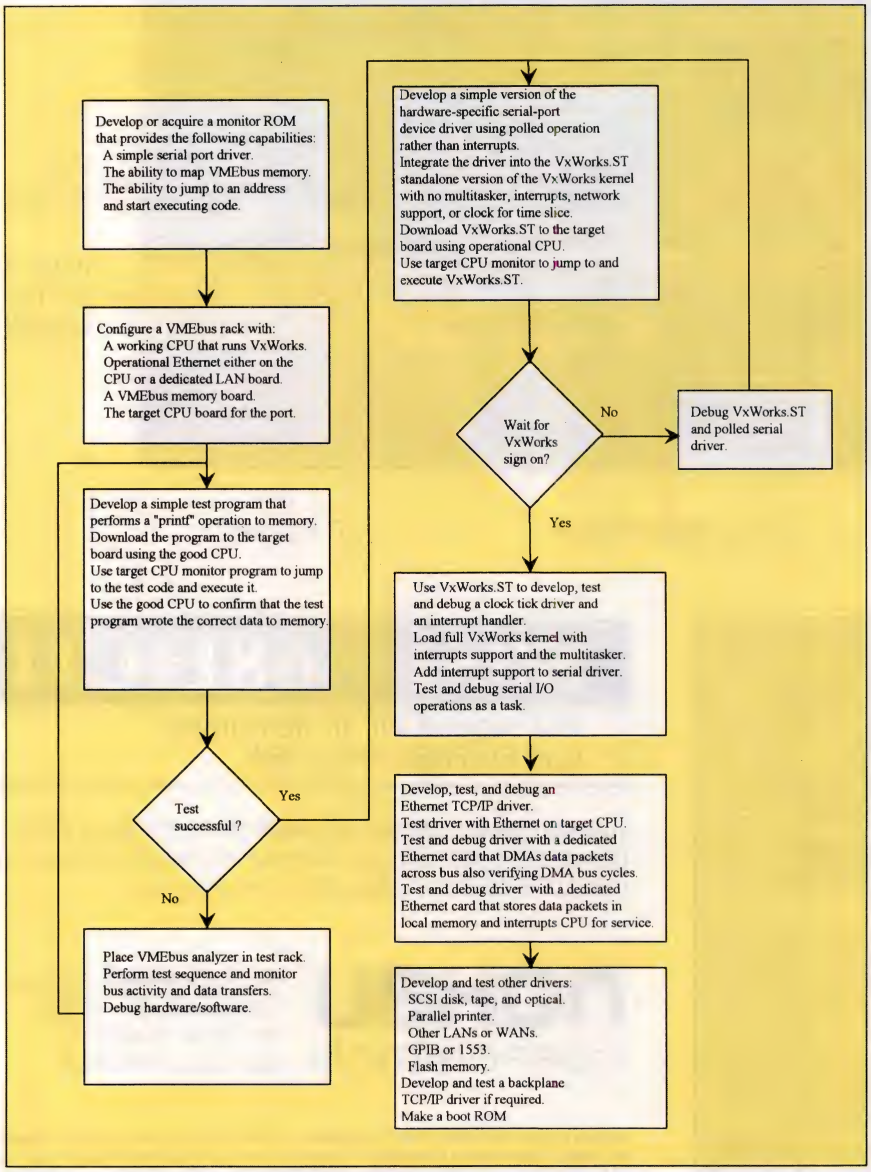
READER SERVICE 101

clock as a part of your hardware initialization code. You can place that code in your driver with little chance of error in actually reading or writing the clock device. But the routines that access the clock could cause problems later, after application deployment.

Recall, for example, that devices like the TIC use a serial interface and thus suffer from relatively slow access. While the TIC causes no problems in the basic operation of VxWorks and OS-9, application software could access the TIC and induce problems. As a result, application developers need to understand the ramifications of reading the hardware clock. For example, the VxWorks port must disable interrupts for nearly 500 μs to allow an application program to read the time from the TIC. The application developer must be cognizant of this time period when the system can't respond to critical external events.

Reading a slow clock is rarely a problem because clock activity typically occurs only in the boot process and hardly ever during time-critical application code.

Once the multitasker is working in your OS, you can proceed to porting drivers. But remember that you're also testing the tasking and interrupt-handling capabilities of the OS as well as the CPU-board hardware that generates interrupt signals for the first time.


Develop or acquire a monitor ROM that provides the following capabilities:
A simple serial port driver.
The ability to map VMEbus memory.
The ability to jump to an address and start executing code.
Configure a VMEbus rack with:
A working CPU that runs VxWorks.
Operational Ethernet either on the CPU or a dedicated LAN board.
A VMEbus memory board.
The target CPU board for the port.
Develop a simple test program that performs a "printf" operation to memory.
Download the program to the target board using the good CPU.
Use target CPU monitor program to jump to the test code and execute it.
Use the good CPU to confirm that the test program wrote the correct data to memory.
Test successful ?
Yes
No
Place VMEbus analyzer in test rack.
Perform test sequence and monitor bus activity and data transfers.
Debug hardware/software.
Develop a simple version of the hardware-specific serial-port device driver using polled operation rather than interrupts.
Integrate the driver into the VxWorks.ST standalone version of the VxWorks kernel with no multitasker, interrupts, network support, or clock for time slice.
Download VxWorks.ST to the target board using operational CPU.
Use target CPU monitor to jump to and execute VxWorks.ST.
Wait for VxWorks sign on?
No
Yes
Debug VxWorks.ST and polled serial driver.
Use VxWorks.ST to develop, test and debug a clock tick driver and an interrupt handler.
Load full VxWorks kernel with interrupts support and the multitasker.
Add interrupt support to serial driver.
Test and debug serial I/O operations as a task.
Develop, test, and debug an Ethernet TCP/IP driver.
Test driver with Ethernet on target CPU.
Test and debug driver with a dedicated Ethernet card that DMAs data packets across bus also verifying DMA bus cycles.
Test and debug driver with a dedicated Ethernet card that stores data packets in local memory and interrupts CPU for service.
Develop and test other drivers:
SCSI disk, tape, and optical.
Parallel printer.
Other LANs or WANs.
GPIB or 1553.
Flash memory.
Develop and test a backplane TCP/IP driver if required.
Make a boot ROM

4. THE PORTING SEQUENCE for VxWorks shows that creating a boot ROM is one of the last required steps. The beginning steps of the porting process aim to ensure that the target CPU can read and write local memory and VMEbus memory.

PORTING DRIVERS

The porting process for OS-9 and VxWorks once again diverges at the driver development phase. With VxWorks, you need to work on an Ethernet driver immediately so that you can begin using the full VxWorks development environment. But Ethernet drivers are inherently more complicated than other I/O drivers, such as a SCSI driver for disk I/O functions, because the LAN driver must handle a network protocol (typically TCP/IP). Therefore, unless your OS architecture dictates otherwise, your next step could well be a SCSI driver.

Developing a SCSI driver for a state-of-the-art real-time OS consists mostly of writing the low-level code modules that interface with the SCSI interface IC. Almost all OSs currently integrate support for SCSI devices, so you typically receive the code that generates command blocks for the most popular types of SCSI devices (disk and tape drives and so forth). For example, OS-9 includes file managers for disk and tape drives that are referred to as the RBF (Random Block File) manager and the SBF (Sequential Block File) manager, respectively. The managers configure generic SCSI command blocks and depend on the device-specific driver to transfer the commands and handle data packets.

The low-level driver needs a few basic capabilities, including data transfer and the ability to distinguish the structure of SCSI command blocks. It also needs to use the knowledge of the command block structure to control the SCSI IC without interrupting the host. For example, the drivers must be able to detect a busy device and retry any operation on its own—without interrupting the host because of an error.

Two other factors help simplify the driver-development task. As noted, you can usually acquire a sample driver developed for the SCSI IC. Smart SCSI ICs can even handle such events as conflicts caused by a

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busy bus without help from the driver. For example, the V4D uses the NCR 53C710 SCSI I/O processor. The IC can directly execute scripts that define complex SCSI sequences without driver assistance. Consequently, a 53C710 driver primarily needs to translate high-level command blocks into scripts for the processor.

When developing a driver for a new or custom SCSI IC, it helps to use a similar sample driver as a guide. For example, you could encounter a SCSI controller in an ASIC that was a part of an ASIC vendor's cell library. That controller would likely be modeled after an off-the-shelf controller IC.

SMART ICs

Every generation of SCSI ICs is smarter than the previous one. This intelligence creates a potential hazard, though, when you try to model a driver after a similar sample driver—for example, if you have a driver for one IC in NCR's 53C700 family and need a driver for another family member. Specifically, consider the differences between the 53C700 and 53C710 devices. The design of both ICs are based on the powerful script language that matches the structure of SCSI command blocks, but the implementations differ in a way that makes drivers for the two substantially different. The 53C700 needs 32 kbytes of script memory in system dynamic RAM because it doesn't support table-indirect addressing. Therefore, the driver must have separate code modules to address each of the eight possible SCSI addresses (or IDs) and each of the eight possible LUNs (logical unit numbers) that can be associated with each ID.

In contrast, the 53C710 device needs only 1 kbyte of dynamic RAM for script memory because it can handle table-indirect addressing that allows one code module to serve all IDs and LUNs. Recognizing such differences in a sample driver and target hardware can save time in driver development.

ETHERNET DRIVERS

While you may not need a Ethernet driver for an OS like OS-9, you need one for VxWorks targets even if its only use is application-software development. In general, Ethernet drivers are more complicated than SCSI drivers for a couple of reasons. First, the Ethernet driver (or, more correctly, the network driver because Ethernet actually refers to a lower-layer data-transmission scheme) must include support for some network protocol—typically TCP/IP. The protocol software handles packetization of data and ensures reliable transmission.

The second factor that complicates network drivers is the asynchronous nature of network communications. A network driver has no warning that data is coming over the network before the interrupt, which causes the CPU to swap to the network driver.

Developing a network driver would be an enormous task if you had to write the protocol software. Most OSs include support for the standard TCP/IP protocol or offer it as an option. The driver development project, therefore, consists mainly of adapting a sample driver to your target hardware. What's more, you are assured of finding a sample driver for the IC on your target among the handful of Ethernet ICs.

Still, you need to match the driver to your target system architecture, specifically how the network IC is implemented in your system. The V4D, for example, has the Intel 83596CA Ethernet IC on board; the IC includes a DMA controller to transfer data packets directly to or from the target's main memory. Other ICs require the CPU to move data, and your system application could even make you choose to implement the 82596 with the CPU in charge of transfers.

You may encounter a system with Ethernet implemented on a separate board and need to address the board through the VMEbus. Furthermore, the dedicated Ethernet board could include DMA capabilities or require the CPU to transfer data. In fact, the recommended porting sequence for VxWorks includes developing drivers for both types of external Ethernet cards as well as an on-board interface. By developing all three drivers, you can also test host CPU- and slave-initiated burst data transfers.

Driver development consists mostly of implementing data-movement routines and formulating the interrupt service routine and routines that interface to the target Ethernet IC. Routines that transfer data for an on-board controller are relatively simple, while routines that transfer data across an external interface (e.g., the VMEbus) vary in complexity based on the bus interface device.

For the V4D, the bus interface code is no different than code that addresses local memory. The V4D uses the Cypress VIC64 IC as a bus interface. The VIC chips are initialized early in the boot process so that the V4D multiported memory can be mapped onto the shared-memory VMEbus at a specific address. Furthermore, a external Ethernet card acting as an Ethernet slave would be similarly mapped onto the bus. The VIC chip handles all bus-transfer overhead, such as arbitration, so the target CPU or a slave Ethernet board can simply read and write memory across the bus.

Of course, different bus-interface mechanisms could greatly complicate the driver. For example, bus-interface ICs that implement message-passing protocols require a driver to use the protocol to transfer data to an external Ethernet card.

If, by chance, you can't find a sample driver for your target OS and network IC, you can still avoid starting from scratch by obtaining a driver for an OS with a similar structure. For instance, no sample driver existed when Heurikon had to develop an Ethernet driver for LynxOS and the 82596 IC. But LynxOS and VxWorks use a symmetrical driver structure. Consequently, Heurikon used the device-specific code developed for the VxWorks driver to accelerate development on the LynxOS port.

BACKPLANE DRIVERS

Most likely, you will have to develop a few more drivers than serial, SCSI, and Ethernet drivers. The popularity of the Centronics-compatible parallel interface, for example, resulted in the interface finding its way into many embedded applications. Yet porting a parallel-interface driver is simple, because the

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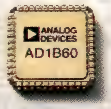

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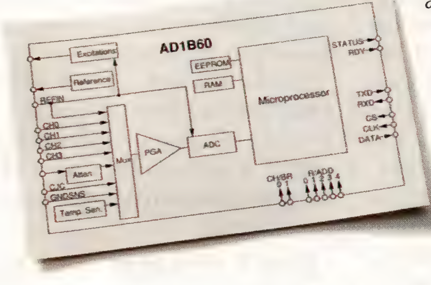

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READER SERVICE 154

hardware interface is nothing more than a parallel port. And matching sample code to any hardware configuration is straightforward.

You also will likely write a backplane driver because embedded systems are increasingly employing the high-level TCP/IP protocol to connect multiple processors via a medium like VMEbus rather than Ethernet. Such backplane drivers provide a standard means of interprocess communications, thereby simplifying multiprocessor system design.

Early backplane drivers were largely custom jobs. But spurred on by the proliferation of the technology pioneered in VxWorks, most OS vendors include backplane driver support for a reference design. Developing a backplane driver will likely be the most complex driver you develop in a system. The complexity comes partly from use of a protocol like TCP/IP but largely from the diversity of bus-interface circuitry.

For example, in its 68040 porting package, Microware supplies a backplane driver for a reference board. But the driver is useful only with boards that use Motorola's VMEbus interface circuitry. While you could develop a driver for other ICs like the standard VIC family, the driver might not communicate properly with the reference driver. As a result, for backplane drivers, the OS vendor should provide the media-access architecture for each bus-interface device and ensure interoperability of boards from different vendors.

VxWorks offers a more robust, if not perfect, set of reference drivers for backplanes because backplane drivers were first used in this OS. You can port a VxWorks backplane driver to the VIC64 IC with little trouble, for instance. But the VxWorks reference driver doesn't take full advantage of all the VIC chip's capabilities. For example, VxWorks supports a single mailbox associated with each VMEbus board, but the VIC chips provide eight mailboxes per board. The VIC chips also include six interprocess communication registers not supported by the VxWorks backplane driver scheme. You can add support for any bus-interface features in a custom driver, but your driver won't necessarily interoperate with other VxWorks targets. Therefore, your target application and interoperability requirements are key to how you implement a backplane driver.

Other drivers that you may be faced with developing include other local- and wide-area-network drivers, GPIB drivers, and drivers for specialized interfaces, such as the 1553 serial interface used in military applications. You should identify the need for such drivers early in your system planning stage because the availability of a driver could well be a factor in selecting a real-time OS.

Even if an exact driver isn't available, some OSs make development of all new custom drivers simpler than others. OS-9's porting package, which includes the source code for all drivers, enables you to match an available sample driver to the requirements of a new device. If your application requires a GPIB driver, for example, you can start with a SCSI device driver because both classes of interfaces are based on parallel data transfers, defined command structures, and bus-arbitration requirements.

TESTING AND COMPLETION

Having completed the port, you can proceed to test all of the OS facilities. Many OS vendors even supply a test suite. VxWorks, for example, includes such a test suite, yet generic test software can't exercise all hardware in a target system.

You should be able to test the SCSI driver thoroughly by using various devices, including magnetic and optical disk drives as well as tape drives. Make sure that you test all interface types that your target supports because SCSI offers many options in the interface specification. For example, test a basic 8-bit SCSI-1 device as well as 16- or 32-bit SCSI-2 devices. And test the operation at fast synchronous speeds if your target supports this type of capability. Bugs in the driver, especially in the interrupt service section, are much more likely to occur at higher speeds.

A rigorous test of the network drivers is also critical. In fact, an example can demonstrate how thorough testing can find bugs traced back to a basic hardware initialization routine. An OS-9 Ethernet driver developed for the V4D showed no bugs upon initial testing. The CPU board sent and received packets flawlessly at a pace typical of many such applications. But when tested on a fully loaded network and asked to handle many small packets, the driver developed errors. Likewise, the driver couldn't handle the transfer of large data files without errors.

The Ethernet driver, as it turned out, wasn't at fault. Instead, the hardware initialization routine executed at boot time caused the problem by setting up the VIC chip improperly. Besides handling the bus interface, the VIC chip can also channel on-board interrupts to the CPU. Therefore, the interrupt signal from the V4D Ethernet controller is connected to the VIC IC, which channels the interrupt to the proper CPU interrupt line.

The VIC IC offers substantial flexibility in how interrupts are handled. In one example, the VIC IC can be programmed to interrupt the CPU based on a level-sensitive or trailing-edge-sensitive trigger. By configuring the VIC for level-sensitive operation, the hardware initialization routine caused the Ethernet driver to lose data. When debugging drivers, remember to look beyond the obvious and recall every byte of code you developed for the port.☐

David Klann, a senior software engineer with Heurikon Corp., has served as a software engineer for the past eight years.

Steven Schultheis, the principal VxWorks software engineer for Heurikon Corp., received bachelor's and master's degrees in astronomy-physics, mathematics, and applied music from the University of Wisconsin.

David Smith, a BS-ECE from California State Polytechnic University, Pomona, currently runs ICON Engineering, an OS-9 consulting house in Minneapolis.

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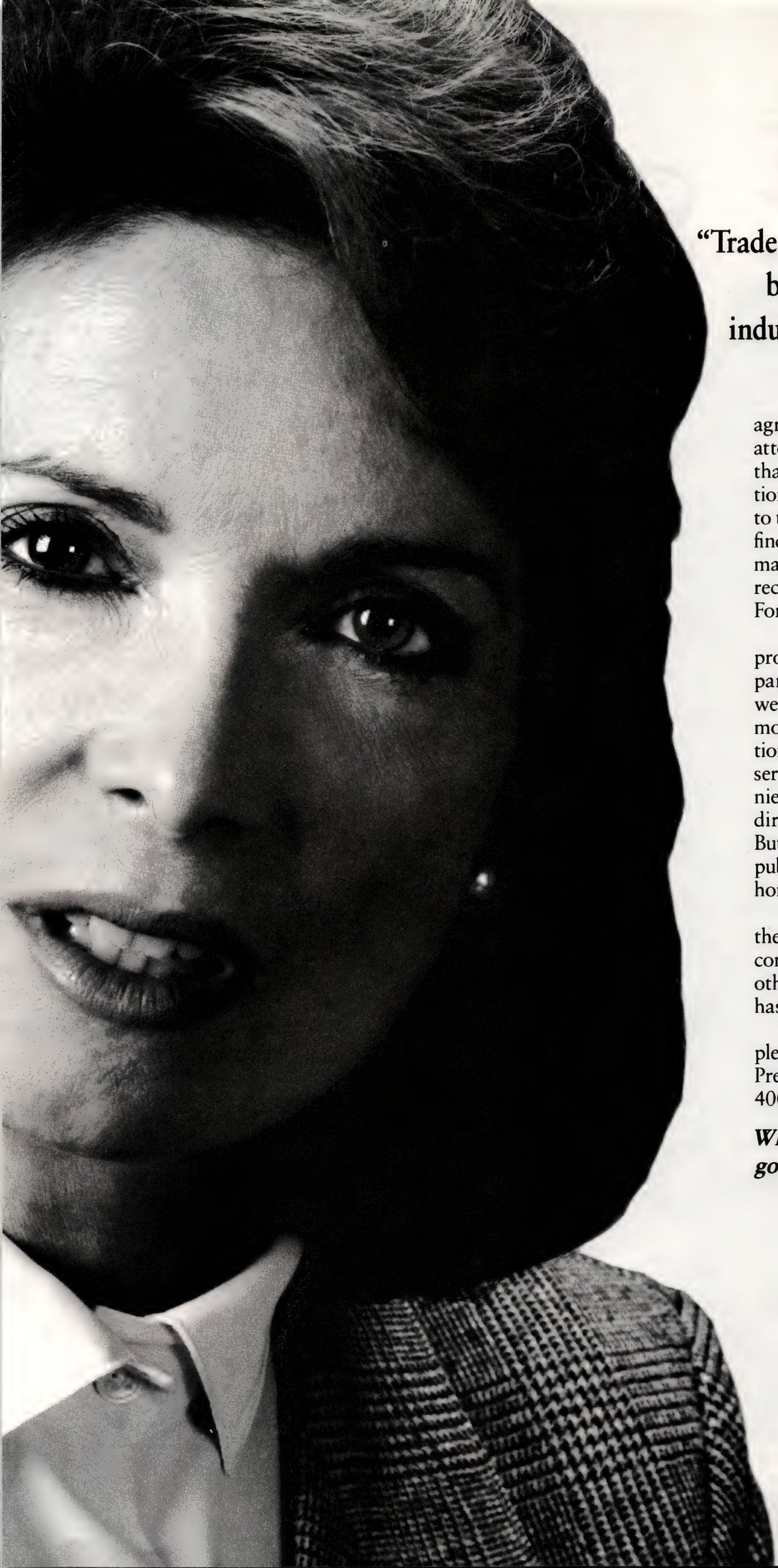

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CIRCLE

521 Generate Varying-Width Pulse Groups

S.R. KAUL, I.K. KAUL, and R.KOUL
Bhabha Atomic Research Centre, Nuclear Research Laboratory,
Trombay, Bombay, India 400 085.

Pulse groups can be generated with sequentially incrementing/decrementing widths using this circuit *(see the figure)*. Looking more closely at the setup, it can be seen that it's based on the use of the digital delay generator (DDG) type AD9501 (the AD9500 can be used for fast pulse applications).

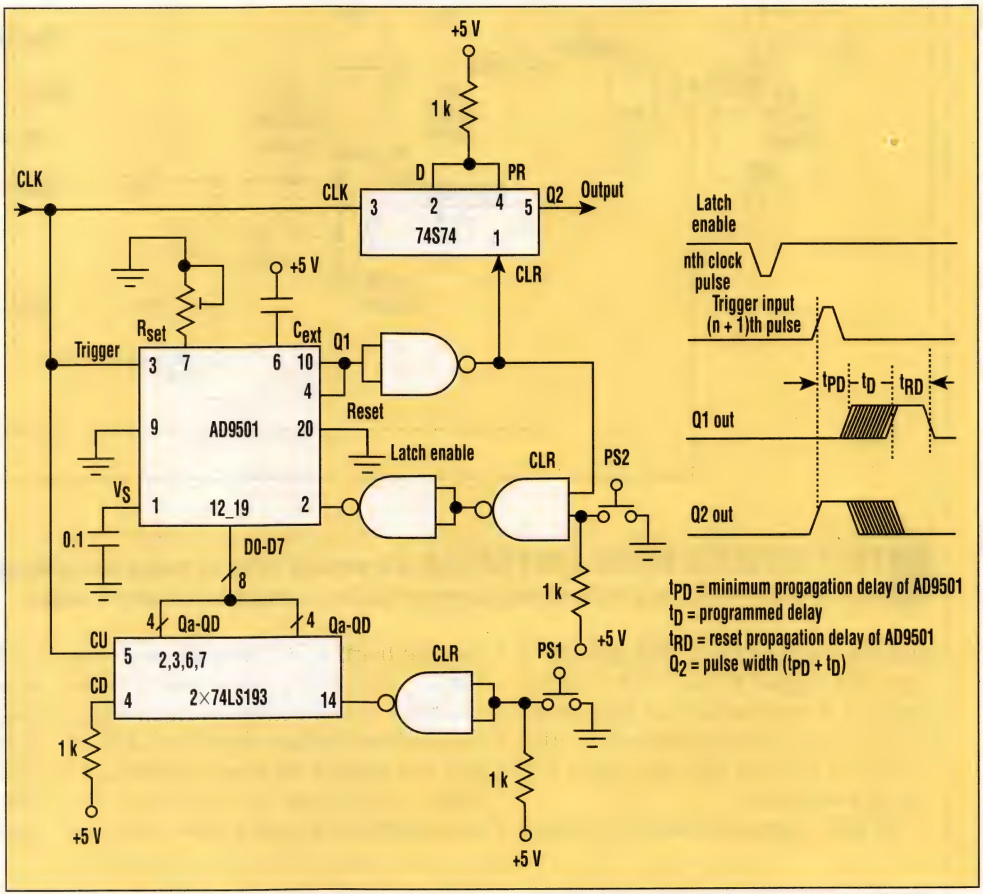
The two counters (74LS193s), wired to count up (CU), are reset with the push switch PS1. Their outputs (00_H) are initially latched on the DDG by the push switch PS2.

The rising edge of the input clock pulse sets the flip-flop, increments the counters (for the next cycle), and triggers the DDG. The DDG delays the output pulse by a time interval that has a value dependent on the preset pulse count, which is 00_H for the first input clock pulse. At this initial count setting, the delay is determined only by the minimum propagation delay (t_{PD}) of the DDG. Simultaneously, the incremented outputs of the counters (01_H) are latched on the DDG for the next cycle. The full-scale width range is determined by the values of R_{set} and C_{ext} in the circuit.

When the clock pulses are fed in continuously at a fixed frequency, the output pulse widths vary sequentially from a minimum to a maximum value. When acquiring the maximum width corresponding to the counter full-scale value, the pulse width decreases to a minimum as the counters are reset to zero by the next clock pulse. For output pulses with a sequentially decreasing width, the counters may be operated in the countdown mode.

To operate the circuit as a digitally programmable monoshot, the count UP/DN input to the counters may be inhibited after programming for a given width.

Alternatively, the counters can be replaced with an octal DIP switch, which can be used to set the DDG delay. Consequently, the switch can be used to control the width of the output pulse.☐



THE GENERATION of pulse groups with sequentially incrementing/decrementing widths is possible using this circuit. The setup is based on the use of a digital delay generator.

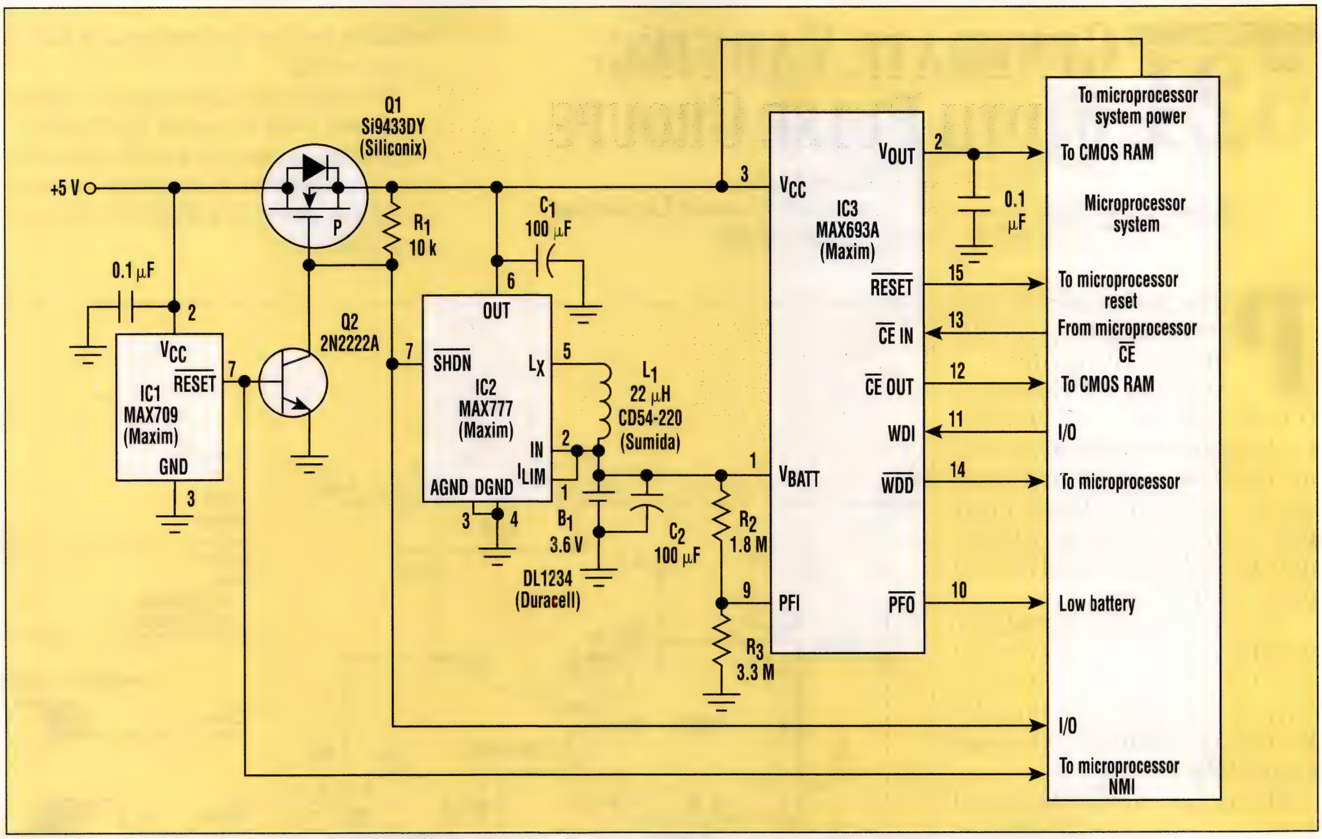
CIRCLE

522 Boost Converter Ups Shutdown Time

DANA DAVIS
Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale,
CA 94086; (408) 737-7600.

Some microprocessor systems require more time for shutdown than that provided by conventional circuits for power-fail detection. Between first warning and the actual loss of power, such systems have extensive "housekeeping" tasks to perform in addition to the memory-write operations that save critical data.

A backup battery and dc-dc regulator can buy extra time for the microprocessor by maintaining V_{CC} at 5 V following the initial warning of impending power loss *(see the figure)*. When V_{CC} falls below 4.65 V, micro-



THIS SYSTEM'S BOOST CONVERTER (IC2) derives 5 V from the backup battery during the brief interval between a low-V_{CC} warning and power fail. As a result, the microprocessor has time to complete its shutdown routine.

processor-supervisor IC1 issues a logic-low signal at pin 7. This signal applies a nonmaskable interrupt (NMI) to the microprocessor. It also turns off Q1 (via Q2) and pulls IC2 out of shutdown.

As the microprocessor shutdown routine begins, IC2 quickly restores the V_{CC} line to 5 V, with power from the 3.6-V lithium battery. Even when the battery voltage drops to 2.5 V, it still can supply as much as 200 mA. When the routine is completed, the microprocessor shuts down IC2 via an I/O line, allowing a second decline in V_{CC}. At 4.4 V, the microprocessor-supervisor IC3 enters its normal battery-backup mode. If desired, separate batteries can be connected for the boost converter and for RAM backup.☐

IFD WINNERS

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Jim Williams, Linear Technology Corp., 1630 McCarthy Boulevard, Milpitas, CA 95035. His idea: *"Create Efficient Laser Power Supply."*

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Geoff Drummond, Advanced Energy Industries, 1825 Sharp Point Drive, Fort Collins, CO 80525. His idea: *"Simple RS232 Sync To Async Converter."*

CIRCLE 523

VERIFY CLOCKS SIMPLY

C. SHANKAR
Indian Telephone Industries, Bangalore-16, India.

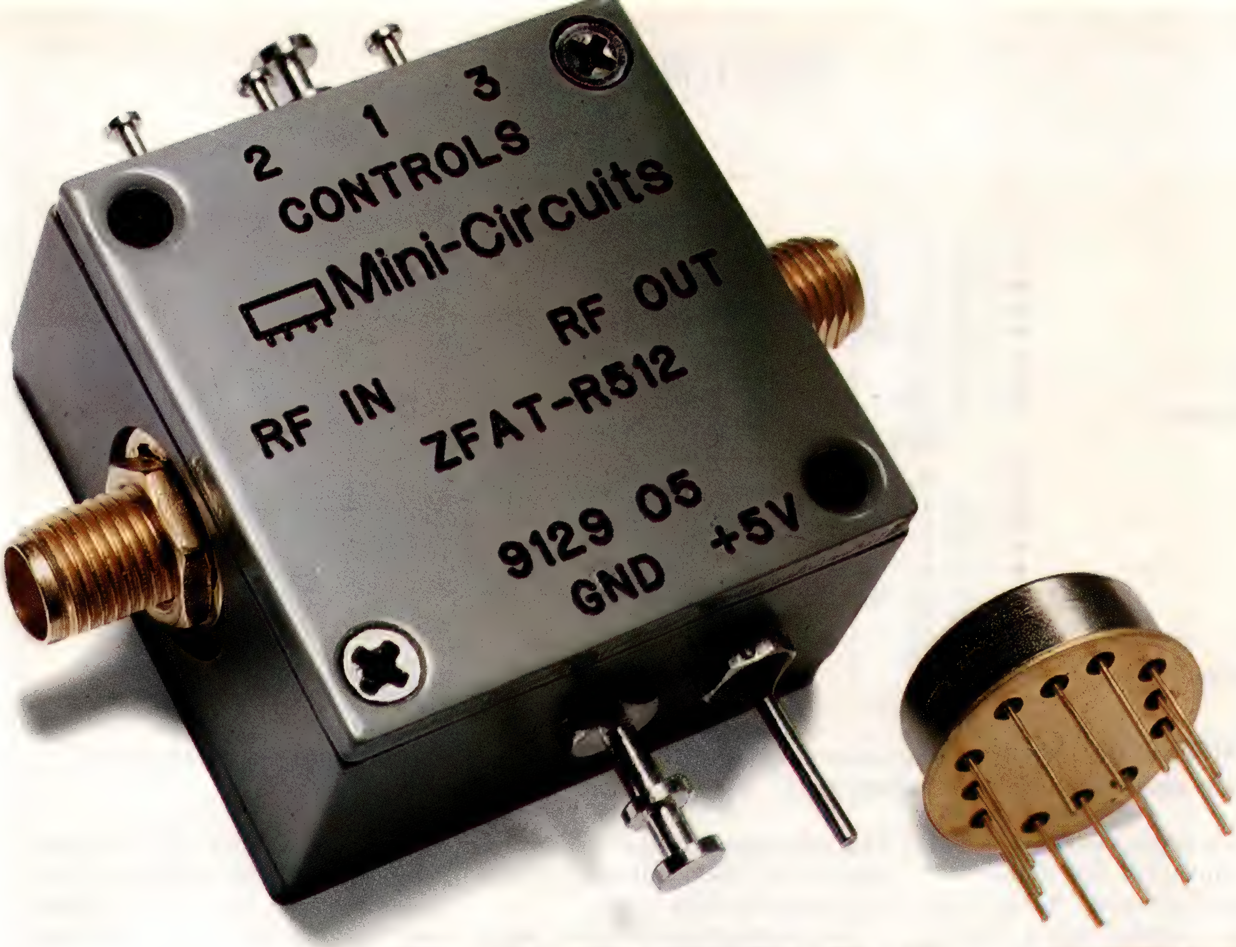
Two clocks can be verified if they are derived from a single source using the simple circuit shown *(see the figure)*. If the clocks do not match in frequency or phase, the circuit generates an interrupt signal.

The setup consists of two 4-bit 74HCT161 binary counters (U1 and U2) whose terminal count outputs are connected to a 74HCT86 XOR gate (U3A).

The clock to be verified (CLK1) is connected to one of the 4-bit counters. A reference clock that is derived from the same source is connected to another 4-bit counter.

The overall idea is that if the clocks are equal in frequency and phase, the counters will generate terminal counts (at RCO) at the same time. This causes the output of the XOR gate to go low.

If the frequency and/or the phase mismatch, the terminal counts are generated at different times. This



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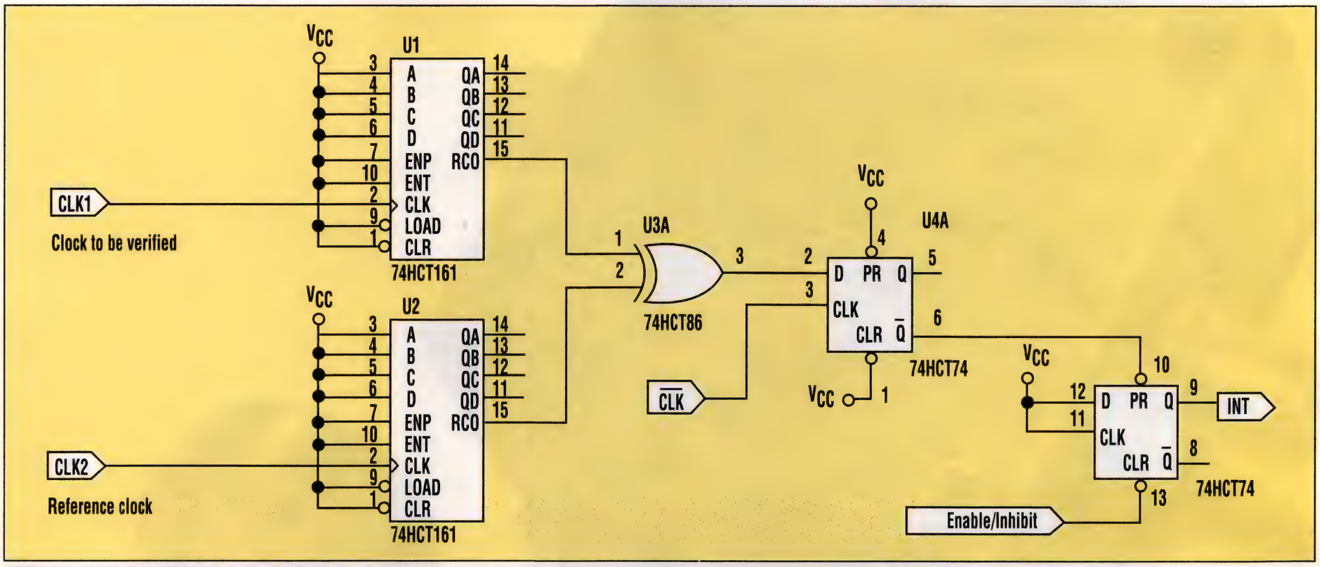
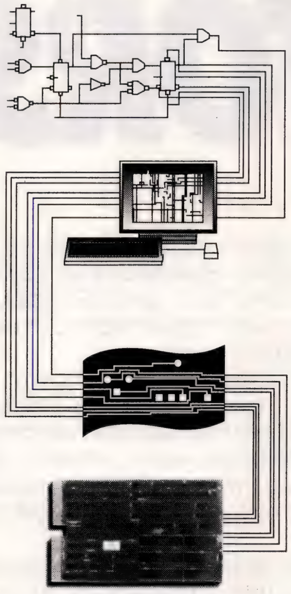


CONSISTING OF TWO 4-BIT binary counters whose terminal count outputs are connected to an XOR gate, this circuit can verify two clocks, assuming they're derived from a single source.

mismatch in timing will cause a high at the output of the XOR gate.

The high "no match" status of the XOR gate is latched into a flip-flop (U4A) at the next edge of the clock. This arrangement takes care of the skew in the clocks, allowing a skew of up to half a clock cycle.

The mismatch in the clock is registered by flip-flop U4B, which raises an interrupt signal. The interrupt output then can be cleared in the interrupt service routine by making the flip-flop's Enable/Inhibit pin go low.□



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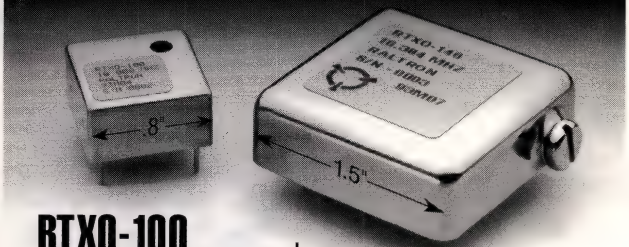

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ELECTRONIC DESIGN QUICK LOOK

EDITED BY SHERRIE VAN TYLE

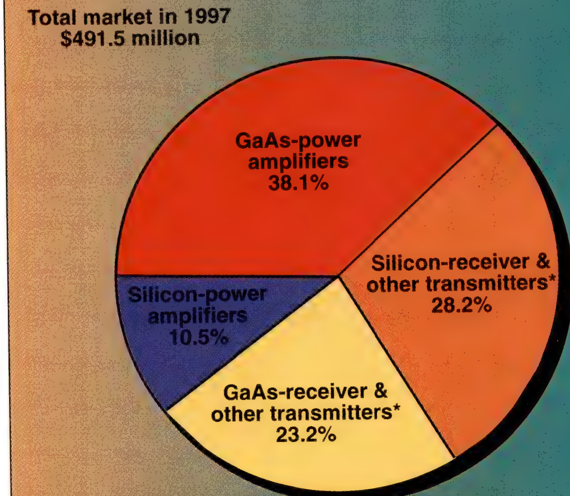
MARKET FACTS

The market for ICs that go into mobile wireless communication products is expected to grow from $26 million in 1992 to about $492 million by 1997. Further, the market is predicted to expand to about $989 million in the year 2000, according to a market study from Venture Development Corp. entitled *The World Market for Front-end Radio/Microwave Monolithic Integrated Circuits in Mobile Wireless Communications Products.*

Application markets studied were cellular phone and data transceivers, cordless and wireless PBX handsets, pagers, personal communicators, and personal digital assistants, data transceivers for specialized mobile radios, portable data collection terminals, and wireless local-area networks (LANs).

In wireless transceiver applications, gallium arsenide supplies lower noise and higher power efficiency, especially at low power source voltages. Yet silicon offers lower cost circuits. Silicon technology tends to be more applicable to lower frequency applications, gallium arsenide to higher frequencies. The Natick, Mass., market researcher estimates that in 1997 shipments of transceiver power amplifier chips will amount to about $239 million; 78% of that is expected to be implemented in gallium arsenide. In contrast, shipments of receiver and other transmitter chips for the transceivers are forecast to reach $252.5 million for 1997, with 55% expected to be implemented in silicon.

HOW MARKET WILL SHAPE UP FOR MOBILE WIRELESS ICs



* Exclusive of power amplifiers

Source: Venture Development Corp.

QUICK NEWS

Intusoft, based in San Pedro, Calif., has set up a Spice bulletin board service (BBS) on the CompuServe Information Service. The free Spice BBS contains Spice models, technical application notes, software utilities, and demonstration software. Engineers can find the bulletin board under the CADD/CAM/CAE Vendor forum on CompuServe. Messages may be exchanged with other engineers, and technical questions can be left for Intusoft's technical support staff. For more information on the BBS, call Intusoft at (310) 833-0710.

The VHDL International Internet Services (VIIS) is an electronic information service for public use and access. The service, which is provided and supported by Menlo Park, Calif.-based VHDL International (VI), is offered through the "vhdl.org" machine connected to the Internet. Basically, the system was set up to provide a focal point for standards activities in an electronic forum, and to disseminate information about VHDL activities such as VI Users' Forum (VIUF) local-chapter meetings, VIUF conferences, survey results, and discussion groups. Vhdl.org is available to related users groups and standards organizations. These other groups manage their own e-mail-based discussion groups and file-repository systems, form news-discussion groups, and so on. For more information, call VI at (800) 554-2550 or (415) 329-0578.

HOT PC PRODUCTS

An electronic technical support center (ETSC) from DiagSoft supplies automated technical support to indiviudal and corporate PC users and to PC original equipment manufacturers (OEMs). In the first service, when a subscriber or owner of the QAPlus software reports a problem to DiagSoft, diagnostics are done over a modem. Next, the process will be automated for users of DiagSoft products, with access to the support center by pressing a help key. Later this year, the company hopes to expand from the current hours of 8 am to 5 pm, Monday through Friday, PST, to 24 hours a day. Contact DiagSoft Inc., 5615 Scotts Valley Dr., Suite 140, Scotts Valley, CA 95066; (408) 438-8247. CIRCLE 461

Power Japanese for Windows 2.0, now on CD-ROM, has a 10,000-word online dictionary and a Japanese language text editor; users can tailor the course to suit their best learning method and, with a sound card, record and compare their pronunciation with that of native Japanese speakers. Like version 1.1, the self-paced upgrade relies on digitally recorded sounds, animation, and drills to teach the most important elements of Japanese syntax and grammar. List price for the software on disk or CD-ROM is $389. Contact BayWare at 1720 S. Amphlett Blvd., Suite 205, San Mateo, CA 94402; (415) 312-0980; fax 578-1884. CIRCLE 462

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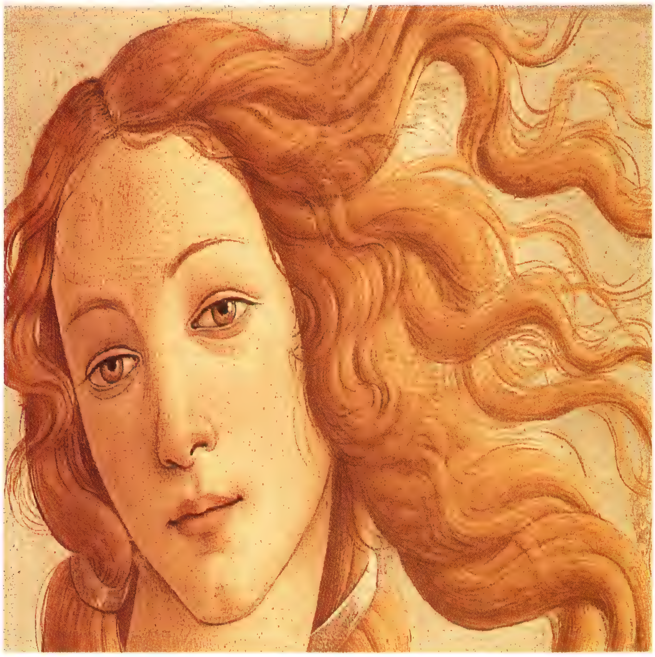
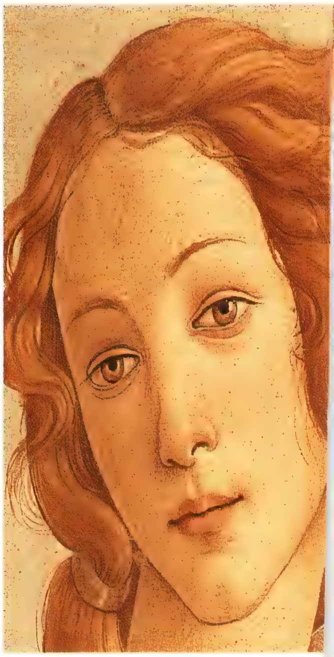
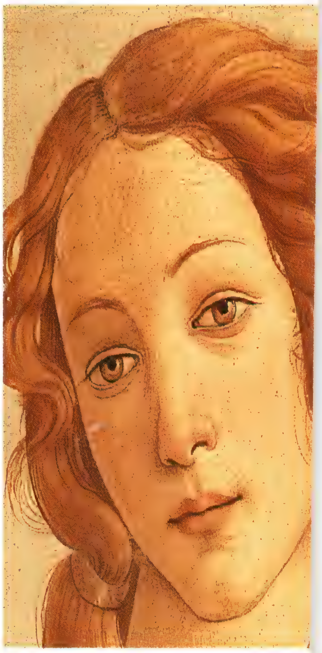




NOT THE SAME OLD WAVE



The same old wave of analog I/Cs just won't cut it anymore — what with the emergence of pocket-sized personal electronics, communications superhighways, and automobiles made more of silicon than metal. That's why National Semiconductor is introducing a bold, new generation of analog solutions guaranteed to help you meet the design challenges of the digital future. Solutions built to deliver the tightest specs you'll find anywhere. You see, we want to be the supplier you look to for all your analog needs. So, the next time you're faced with a really tough analog problem, give us a call. Or simply turn the page. And see for yourself why we're **not the same old wave.**

OFFERS YOU CAN'T REFUSE

A report outlining progress in implementing the administration's civilian technology policies is available on paper or by the Internet. The 68-page document, "Technology for Economic Growth: President's Progress Report," derives from the Technology Summit sponsored by the Berkeley Roundtable on the International Economy.

The paper document (PB 94-107430) is available for $15.50 from The Department of Commerce, National Technical Information Service (NTIS), Springfield, VA 22161; (703) 487-4650 or through the Internet (telnet fedworld.gov).

EYE ON ISO 9000

Siliconix has received ISO 9001 certification for its semiconductor design, development, and production facilities in Santa Clara, Calif. The Santa Clara, Calif. company manufactures semicocductor products for switching, motion control, and power supplies. The company is a member of TEMIC, the microelectronics arm of the Daimler-Benz Group. The company's address is 2201 Laurelwood Rd., P.O. Box 54951, Santa Clara, CA 95056-0951; (408) 988-8000; fax 970-3950.

CIRCLE 463

IBM Corp.'s processes in six of its software manufacturing sites have meet ISO 9000 standards for manufacturing, product design, and servicing operations. The sites are Tokyo; Copenhagen; Sydney, Australia; Boulder, Colo.; Charlotte, N. C.; and Kingston, N. Y. Contact IBM Corp., IBM United States, 1133 Westchester Ave., White Plains, NY 10604.

CIRCLE 464

A designer and manufacturer of wire and cable products, Belden Wire & Cable Co. has achieved ISO 9000 registration for its engineering and manufacturing facilities in the United States. The six Belden manufacturing plants registered under the ISO 9000 standard are Clinton, Arkansas; Essex Junction, Vermont; Franklin, North Carolina; Monticello, Kentucky; Richmond, Indiana; and Tompkinsville, Kentucky.

These plants produce multiconductor, coax, cords, leader wire, fiber optics, and flat cable. For further information, contact Belden Wire & Cable Co., P. O. Box 1980, Richmond, IN 47375; (317) 983-5200.

CIRCLE 465

KMET'S KORNER

...Perspectives on Time-to-Market

BY RON KMETOVICZ
President, Time to Market Associates Inc.
P. O. Box 443, 100 Prickly Pear Rd., Verdi, NV 89439; (408) 446-4458; fax (408) 253-6085

Missing the staffing ratio was shown to produce business profitability misfortune. But product developers are human and they will error on the realization of a unity staffing ratio. This column further examines the composition of the commitment term to identify its tolerance to error and its upper limit.

Work quantity/commitment = duration

First, a reference work commitment figure is needed to keep the system stable. This number is commonly referred to as the hours per week worked by new product developers. It's a personal number—some work close to the societal norm of 40 hours per week and others work significantly more. In all my days on the job and in all the companies where I consult, rarely have I experienced or witnessed a new product developer working a 40 hour week—it's usually more like 45 to 50 hours. But let's get to planning. To do rapid new product development, an organization has to know, in detail, and manage work commitment being put forth by the new product development staff.

As a starting point, let's say that a reference new product developer works a 40-hour week. With this point set, a staffing ratio equal to 1 implies that his limit is not exceeded. Should product developers work beyond the reference, the staffing ratio is adjusted upward in proportion to the increase in effort. For example, working a 50-hour week as compared to a 40-hour reference gives an adjusted staffing ratio of 1.25 (1 + 10/40). Working an 80- hour week gives an adjusted staffing ratio of 2.0 (1 + 40/40). As the adjusted staff ratio goes up, it suggests that new product developers are working longer days and weekends to beat time-to-market goals set when the staffing ratio was equal to one.

In tabular form, working more to get done sooner looks like this:

Weekly hours	Commitment	Daily hours	Weekend hours
40	1	8	0
50	1.25	10	0
60	1.50	12	0
70	1.75	12	10
80	2.00	12	20
90	2.25	14	20
100	2.50	15	25

It's easy to work a lot; in fact, it's easier to work more than to work less. Extend the workday by two hours and it's a 50-hour week; extend it by four hours to put in 60 hours a week at the job; add a long Saturday to accumulate 70 hours; and then take some work home to add up even more hours. Whew!

The limits of commitment are now forming—it cannot exceed 2.5 for physiological reasons; it cannot exceed 1.75 on a sustained basis for psychological reasons; and operating between 1 and 1.75 becomes a matter of personal choice. From an organizational perspective, undercommit by 50% and the time-sensitive product development effort becomes a business flop. Overwork the development team by 100% to get the same result for a different reason. Striving to work below a normalized commitment of 1.5 usually gives the business and personal win-win that organizations desire.

More information on this topic is contained in New Product Development: Design and Analysis, which can be obtained by calling Time to Market Associates.

DID YOU KNOW?

. . . that a survey of 4000 designers from around the world shows that 71% of respondents use multiple VHDL tools, showing that the VHSIC Hardware Description Language is being used in several phases of designing. Further, 100% of the respondents indicated that they are using VHDL for simulation; 76% said they also use VHDL for synthesis. Also, 82% of users indicated that tool quality is good to excellent; 18% responded that tool quality is fair or poor.

Source: VHDL International Inc., (800) 554-2550; (415) 329-0578. For a survey summary, send the e-mail message "send vi/survey result93.txt" to "archive@vhdl.org."

MY VIEW

...The opportunity short shrift

BY FRANK J. BURGE
Director of Market Development for Electronic Design

In many communities the quality of the neighborhood is defined by the quality of the local school system. Living in a neighborhood with great schools not only supposedly provides your children with an education advantage—it also brings credit to the parents. It's a symbol of cultural elevation.

Last November, the *San Jose Mercury News* carried a front-page story about Pacific Bell's plans to invest $16 billion by the year 2000 on a communications superhighway. The system would offer an entertainment, information, and education menu to satisfy every interest. PacBell is after the $50 to $75 a month the typical American family spends on cable, the telephone, and movie rentals.

The announcement caught my eye because the new system would offer an alternative to the cable company I now deal with. A company that has installed a new system, raised rates, and made it virtually impossible to register a complaint because their lines have been so tied up with calls from irate subscribers. Dealing with the cable company bozos is driving me nuts. So the thought of someday being able to switch to PacBell gave me hope. But wait.

Then I looked at the systems map. Our town of Los Gatos was not included in the system. Suddenly it dawned on me. Maybe it's because our community is served by General Telephone. Not Pacific Bell. Does that mean that our children will miss out on the enriched learning experiences offered to the children in neighborhoods connected to the communications superhighway. What are we supposed to do? Bus our kids to a learning center in a PacBell neighborhood?

How we define the desirability of a neighborhood is about to change. Home values may well be influenced by access to the educational programs offered on the communications superhighway. Home buyers will not only inquire about the local school system but also ask whether the home is connected to the PacBell system. And since Los Gatos won't be connected, does this mean that it will become a disadvantaged neighborhood? Lots of fine, friendly folks and classy antique shops, bars, and restaurants but certainly not a neighborhood that provides the education advantage.

Access to world-class educational programs may just turn the boob tube into the opportunity tube by providing lifetime learning experiences for all of us. But this assumes someone will fund program development and guarantee system access. Just who is going to do that? My barber tells me the odds are against it ever happening. And my barber is one smart cookie.

Since the game is to chase the $50 to $75 a month households spend on cable, the telephone, and TV rentals, how about poor neighborhoods? Will they automatically be redlined out of the system just because settlers in the neighborhood don't have the $50 to $75 a month for the menu? Who decides who gets what?

My guess is that the usual suspects will get the short shrift.

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IEEE COMPUTER MAGAZINE 9/93

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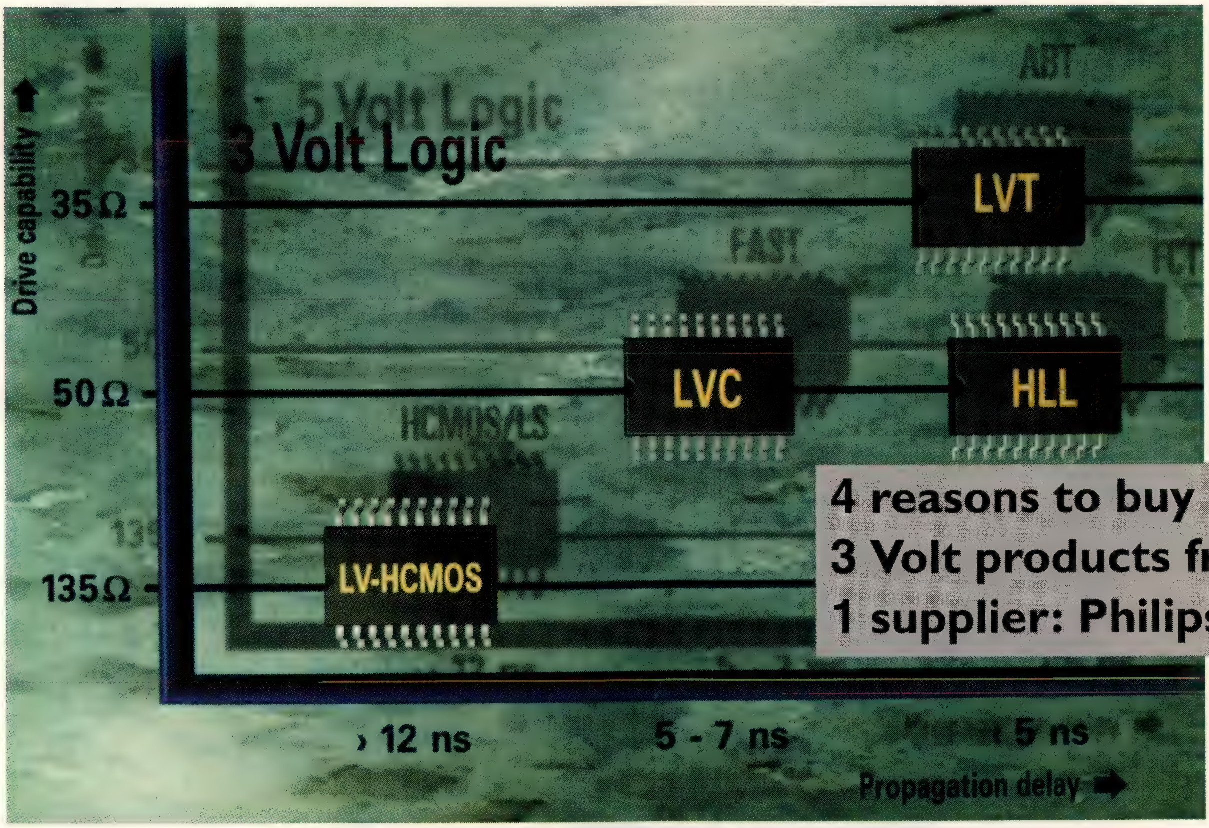

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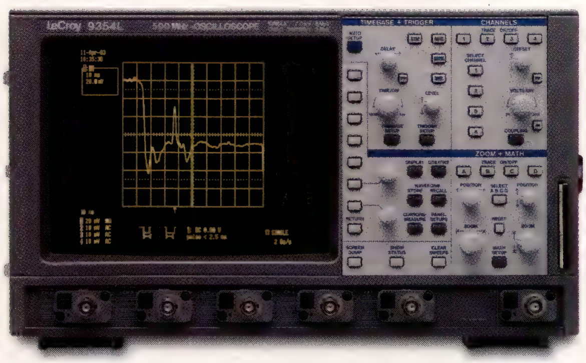

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PEASE PORRIDGE

WHAT'S ALL THIS QUALITY STUFF, ANYHOW?

WELLLL—I have been figuring for years that someday I would write about "quality." But aside from saying that we're all, of course, in favor of the *HIGHEST POSSIBLE QUALITY*, what else is there to say? Wouldn't that make a very short column? Yet despite the truism just listed above, very few of us readers drive a Rolls Royce.

So perhaps we should admit that we're all interested in very good quality at a reasonable price—a Volkswagen or Ford price, maybe even a Cadillac, Acura, or Mercedes price—very good quality, *appropriate* quality, but not necessarily the *highest possible* quality.

BOB PEASE OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

I still recall very plainly that VW used to advertise and brag that they had more QC inspectors than they had cars, and those old VW beetles had pretty good quality. Of course, it might be that the inspectors forced the production engineers to go back and solve the design and manufacturing problems. Maybe that's a back-door way to achieve good quality. Anyhow, I still like my old Beetle, running reliably at 287,000 miles. It's not the highest quality, maybe not as good as a Rolls Royce, but it is *appropriate* quality.

I recollect the story of one of the pioneering transistor companies, back in the '60s. They had agreed to ship to their customers transistors with an AQL (Acceptable Quality Level) of 2%, which was pretty good for those days. So the tester would test 98 good parts and put them in the box. Then, following her instructions, she would add 2 bad transistors to finish off the box, thus bringing the quality to the exact level desired. This went on for some time, until one of the customers got suspicious, because the two bad transistors were always in the *same corner of the box*! Then things were changed....

Now let's get serious. I propose that not everybody really wants to buy parts with the highest quality and the smallest AQL. Let's consider a few practical examples. If I'm testing some gates or flip-flops, the output had better be about right, with a very high confidence, on every test. If I make 20,000 bad dice in 1,000,000, and I only reject 19,700 of them, you as a purchaser might be quite displeased to get an incoming quality rate of 300 ppm. So, it is pretty clear-cut that for ordinary commodity ICs, the parts and the testing should be very good so that no bad parts get to the customers. Many IC manufacturers do well at this.

Ah, but what about precision analog components? Precision op amps, 16-bit DACs, low-noise references? Can they always be tested with full precision and confidence?

What about a high-gain op-amp, such as OP-07? If the output swing is a 10-V step (either + or –), then the maximum input error (delta V) must be less than 50 µV. Further, it must be less than 50 µV with a VERY HIGH confidence level every time you measure it. What if it is 34 µV p-p sometimes when you test it, and 38 µV p-p other times, and 30 µV another time? Then if you see 47 µV on another part, it might change to 51 µV p-p if you test it again, and that would be a fail of the test. So, your testing must be done with good repeatability and low noise.

Is it realistic to try to meet an AQL of 0.01% on such a test? Is it reasonable? Is that what you want to pay for? Would an AQL of 0.2% be just as reasonable? Let's look at another spec. The OP-07A is guaranteed for 0.60 µV p-p of noise voltage, max, in a bandwidth of 0.1 Hz to 10 Hz. When you test an amplifier for noise in a fairly small bandwidth like that, you must not expect to get exactly repeatable results. So if you measure 0.42 µV one time and 0.48 µV another time, you have to be very careful about the repeatability. If there is much *noise*, the guard-bands must get bigger and bigger until the spec is a LOT more conservative than what you're actually measuring. As it is, the OP-07s have 0.35 µV p-p typical, yet we're barely able to guarantee 0.6 µV p-p.

What if we said that this spec was only guaranteed at an AQL of 0.5%? Could we then guarantee 0.45 µV p-p? Would you prefer to buy that as a spec? Would that part be of any significantly lower "quality" than the one with 0.60 µV max? I myself would sooner buy the part with the looser (0.5%) AQL and the tighter spec, as I think it is a more realistic kind of spec with more realistic testing. The yield to the manufacturer might be better, the testing might cost less, and the actual noise performance might be better. What do *you* think? Comments invited.

At one time, one of the major suppliers of precision analog parts used to guarantee reference ICs with a certain long-term stability. In the fine print, they said that 90% of their production would meet that spec, even though they did not test for this. I dunno, but 90% seems a little rough as a quality level. Still, at times, that may be an *appropriate* quality level. But the company has stopped saying that....

Now, I will get into the MEAT of the topic. I recall reading the writings of such people as W. Edwards Deming, Genichi Taguchi, and several other promoters of "quality." They argued that we should not rely on testing for high quality. We should not be trying to "test high quality" into our products, but instead we should build them with such high quality that testing is superfluous. That's what Mr. Deming said, and he was considered "the dean of the quality movement." When I first started writing this column in August of 1993, Mr. Deming was very much alive and kicking, and I was hoping to start a dialog with this feisty old-timer. However, Mr. Deming unfortunately died on December 20, 1993, and I'm disappointed that I cannot duel with him verbally. Still, maybe some of Mr. Deming's colleagues will be in a mood to hold up his end of the arguments, or explain what Mr. Deming thought.

NOW, Mr. Deming's philosophy seemed to say to the entire semiconductor industry: "Do not rely on testing. Just build everything perfect." Well, when we build good op amps, we may get a yield of 80 or 90 or maybe 93% at "wafer-sort," when we probe and test the chips on the wafer. We ink any dice that fail any test, and lots of good dice remain. After we assemble all of the good dice, we test the packaged circuits *again*, repeating many of the tests to weed out anything that may have gone sour, or worsened after assembly, or that may run poorly at a hot or cold temperature. Now we have a yield loss of only 1 or 2 or 3% at this "classification test" after assembly. Still, this is *infinitely* far away from Mr. Deming's philosophy. Why are we semiconductor manufacturers so thick-headed? Why can't we get anything right? Hmmmmm.

If you buy LM324 quad op amps in moderate volume from NSC, you pay about 38 cents and you get 4 good op amps with a quality level of about 99.9996% per package (about 1-ppm reject rate per amplifier). That may not be the best op-amp you can buy, but it's pretty darned good at the price. And I claim that it's the testing that makes these amplifiers so good. If you looked in our "scrap pile," you would find some amplifiers that literally meet the published spec—but we have installed tests to make sure they're rejected. Hey, we reserve the right to reject op amps even though they meet the published specs, because we determined that there's something not quite right about them. Do we get this excellent quality by doing *no* test, or *minimum* testing? *Hell no.*

Ten years ago, we were shipping some of the highest-quality amplifiers in the industry, with an AQL perhaps 99.92%. Pretty good in its day. But we're doing better now—by a factor of 100 or 200. WHY? Because we have better tests. If you took some 1984 op amps and ran them through our 1994 testers, we might pass some that we failed before—because our tests are better. And we would surely fail some that were passed back in 1984—because our testing is better.

Over the past few months, I've asked several friends who work in Quality functions, test engineering, etc., and looked around myself trying to find out the answer to these questions: If the whole semiconductor industry is acting in contradiction to the "no testing" philosophy, has anybody made statements specifically rebutting it? And, has anybody explained that Deming's advice *does not apply* to the semiconductor industry.

As of yet, I haven't found anyone who has ever heard this stated. SO, you're going to hear it right HERE for the first time: There may be many kinds of manufacturing where testing to achieve high quality is the wrong way to do it. But in the semiconductor manufacturing business, testing is *EXACTLY* the right thing to do to get high quality.

NOW, I will not say that testing is exactly the *cause* of the good quality. We design these circuits to be of very high quality, very manufacturable. Our wafer fab usually has excellent quality, so these ICs usually do work well with high yields. But if a run has fewer parts than normal that meet all specs, we don't let that affect the quality of the parts we ship. We do our testing, and the test results tell us what's causing us yield loss.

When we go back to solve a basic design or manufacturing problem that hurts the yield, that may also help the real quality, too. Yet I claim that it's the testing that drives the quality. What kind of IC, or car for that matter, would you buy if you were assured it was so good that no testing was needed?? How would the manufacturer know that the quality really was very good if he did not do tests?

If a Taguchi expert told you how to change your design, but decided not to check his results because his engineering was of such high quality that he didn't have to do any checking, would you buy *that*? NOTE—almost all of our customers are now accepting our testing as quite adequate. So when they buy circuits from us, they do not have to retest them for conformance to the guaranteed specifications at their "incoming inspection." That seems reasonable.

But of course when the customer assembles 22 or 46 or 79 components onto a board, then it's time to do some more testing for that assembly. I recently heard several friends complain about the poor quality of some electronic stuff they bought recently—some made in the U.S.A., and some imported, too. Right out of the box, the equipment failed to work, and you could *tell* that it had never been tested. Are you readers seeing that, too? Are some manufacturers starting to take "no testing" literally? If they talked themselves out of final test, a final *functional test*, that's pretty scary....

I had a talk with Melodie McClenon, manager of our Data Acquisition Test Engineering group. She agreed that we do find it important, occasionally, to add tests. They're necessary to screen out the few parts with bad quality which customers occasionally reject and gripe about. Often, a test is added to guard retroactively against some kind of a "Quality Accident," where a customer finds quite a few parts out of spec. Later, some manager may propose to delete that test as "superfluous." Melodie says she sometimes has to fight like heck to keep the test in, and she can usually do this by proving that the test, while usually unnecessary, is keeping a 1-ppm failure rate from being shipped.

I agreed that, if on most days, the test takes a few milliseconds, and cuts out a 1-ppm reject mode from being

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shipped, and it's ALSO able to help avoid the possibility of some disastrous bad parts from being shipped on 1 day out of 1000, that sounded like good judgment to me. I told her that I was on her side, and if she needed anybody to help her, I would fight like hell for her. It's always good to find a friend with ideas worth fighting for.

I have heard some guys argue that we should improve the yield of our op amps to 100%. I'm skeptical of that idea. At present, we have optimized for the lowest total cost for a good die, including the cost of testing. If we try to optimize the yield, with special wide spacings, special coatings, special processes, special redundant circuits, and so on, we might get a much higher percentage of good dice. But there would be fewer good dice per wafer—and fewer per dollar. Would these fewer dice be of higher quality? Higher reliability? How much better? And, if they are a little better, how much extra would you like to pay for them? Would you like to buy some with no testing? Just think about all of the money you would save by cutting out the testing....

Other people have argued that it's bad to have a low yield, because the quality must be bad. Nobody would want to buy an IC made with a yield worse than 50%, right? *Well*, almost every computer in the world has a processor chip that came out of fab with a wafer-sort yield much lower than 50%. That low a yield would sound pretty dumb for an op amp or gate or counter. But for a big processor, a yield of 10 or 20 or 30 or 40% may be quite rational, and very reasonable compared to making smaller dice with higher yield. It certainly doesn't mean that the dice which pass all tests are of poor or marginal quality. So far, we're doing exactly what Mr. Deming says not to do—yet our quality and reliability keep getting better, and cheaper. And everybody in the Semiconductor industry is doing the same.

One engineer pointed out that to plan to ship a part with the "correct" amount of quality, one might want to know if the intent is to ship a "Yugo," or a "Rolls Royce," or perhaps a "Honda Civic." If we wanted to sell the LM324 as the Yugo of the industry, we could surely increase the yield by shipping parts that just met every published spec—but that might be wrong. The LM324 may have a Yugo level of specs, but we want to make sure it's tested out to a high grade of quality, a "Honda" grade of quality and reliability. Therefore, when you buy one, it comes with some *awfully good* quality. Do you know anybody who actually builds in worse quality on cheaper parts? Our customers, such as H-P, Delco, or IBM, would never stand for that....

Recently, I was surprised to learn that most of the early NSC linear ICs did not have any protective coating of Vapox or Nitride over the die. So, 24 years ago, LM108AHs came with a metal wire just flying through the air above the die, above the aluminum metallization, with no Vapox passivation over the die.

Were those old LM108s and LM101As less reliable than what we make these days? Maybe. But they have shown us a lot of proven reliability. Are new LM308ANs in epoxy mini-DIP packages less reliable than dice in hermetic packages? Well, the new mini-dip ICs are all lead-bonded with automatic machines, with much less variability and better repeatability than the old human-controlled lead-bonders. These ICs are ALL awfully reliable nowadays, and have excellent quality.

(Note, technically we must avoid confusing *reliability* with *quality*. Yes, a part that fails after a customer puts it to work can make the customer just as unhappy as a part that never met spec in the first place. But we have to treat those two problems *separately*. We want to provide parts with excellent quality *and* excellent reliability, and we have to be careful not to hurt one while helping the other. For example, if we do a burn-in test, we must make sure it doesn't harm a part's reliability.)

Now, a great majority of what Mr. Deming said makes excellent sense to me, and I'm pleased to recommend his ideas as an excellent legacy of his career. He observed, for example, that when making cars or airplanes or lawn mowers where the quality is randomly poor, and you're forced to go back and rebuild or replace the engine or the transmission (or the paint) before you can ship the product, it's a LOUSY way to do business.

So, do any readers have any opinions on testing? Have you seen anybody else's good convincing statements or arguments on this topic? I'd love to hear from you. I do know that NSC has always done some testing on every component they shipped, and it's unlikely that we'll change that statement. In fact, *more* testing usually helps provide higher quality, compared to *less* testing.

As a final note, I sent an early letter on this topic to Mr. Deming at his home. He did not reply at that time, but it's not possible to draw any conclusions from that. I just wish I had been able to find a good excuse to talk to him earlier!

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer

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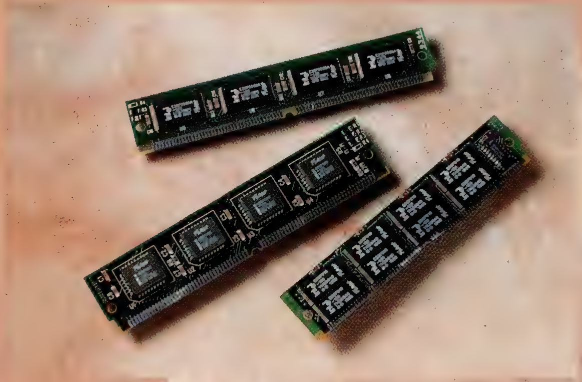

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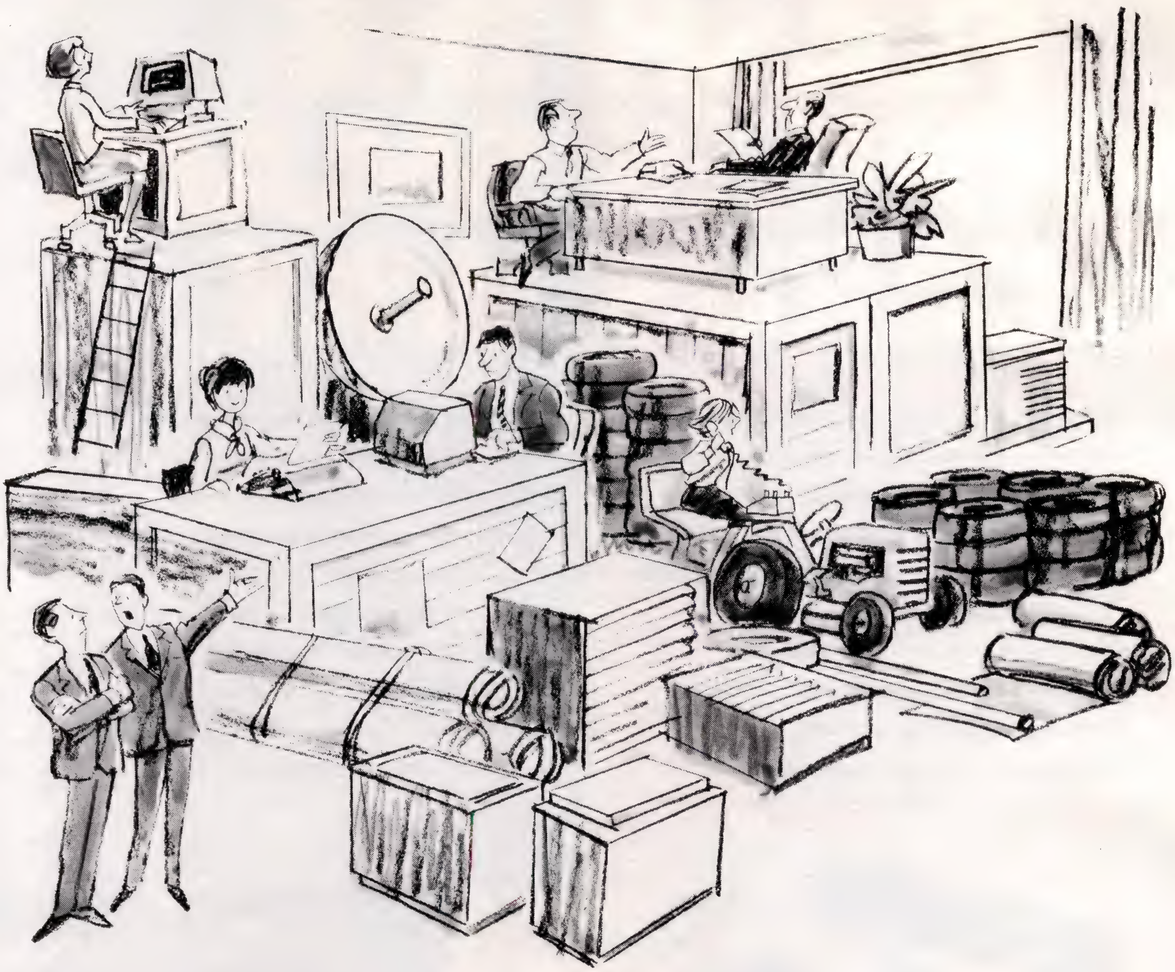

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PLUGGING INTO PCMCIA

PnP IMPACTS PCMCIA

TERRY MOORE AND DANIEL STERNGLASS, DATABOOK INC.

The Plug and Play (PnP) ISA standard, recently developed by Microsoft Corp., Redmond, Wash., and Intel Corp., Santa Clara, Calif., is a component of the PnP initiative, which aims to simplify the configuration of next-generation PCs. It includes both hardware and software elements. Hardware configuration, such as I/O and memory addresses and IRQ and DMA-channel assignments, are under software control instead of being set by jumpers.

All PnP ISA features are available to standard, unmodified ISA bus systems. Hence, although PnP ISA is often described in terms of desktop systems, it's equally applicable to notebook systems, and will be very important for future notebook designs.

PnP ISA support is particularly important for systems that are frequently reconfigured, such as notebook computers connected to docking stations or notebooks with PCMCIA support. Plug and Play ISA offers some inherent advantages for notebook systems, such as how they interface with the docking stations.

At present, the docking station is used somewhat awkwardly. Manually docking or undocking a computer requires a change to the CMOS setup, the CONFIG.SYS file, or the AUTOEXEC.BAT file to reflect the altered hardware environment. This process is error-prone and intimidating to many end users. The PnP ISA standard can eliminate such manual changes.

In addition, the mechanical design of a docking station may result in the notebook PC's PCMCIA slots being inaccessible when the PC is docked. Using Plug and Play ISA, system software can disable the on-board PCMCIA controller and activate a second controller that's actually part of the docking station. Multiple PCMCIA controllers can also coexist.

PCMCIA controllers without PnP ISA support use predetermined I/O addresses for their internal registers. Such addresses may conflict with fixed addresses used by peripherals in a docking station. If the notebook is designed with a PCMCIA controller that offers PnP ISA support, like the Databook DB86084, then the controller's addresses can be relocated to eliminate such conflicts.

Similarly, some PCMCIA cards may require I/O addresses that could conflict with the addresses used by the PCMCIA controller. Again, if PnP ISA support is incorporated into the PCMCIA controller, the controller's I/O registers can be moved to eliminate the conflict.

Because PCMCIA-based I/O devices are starting to proliferate into the industry, next-generation notebook PCs may include more than two PCMCIA slots. Because of IC packaging (pin-count) limitations, this will generally result in a need for multiple PCMCIA controllers. The PnP ISA specification offers a way to support multiple controller chips without dedicating multiple pins or adding external address decoding.

End user's expectations for ease of "hot docking" have been set to a high level by Apple Computer's Powerbook notebook systems. The system software employed by the Powerbook is more integrated than current versions of DOS and Windows. Using the Apple notebook computer, when users prepare to leave the office, they simply copy any new files to the internal hard drive and then undock the system. Resident software automatically responds to the change in configuration, without even rebooting the system.

Similarly, when the user returns, he simply re-docks the system. The intelligent software notices that the additional disk drives and network drives are now accessible, and the icons reappear on the screen. Any new or updated files are then transferred from the notebook. In many cases, DOS-based applications bypass the operating system when accessing the hardware and the hardware in the DOS/Windows systems can not be fully reconfigured under software control.

With the built-in hooks in Apple's hardware, the software can manage the system's configuration. The PnP ISA standard gives the same advantages to DOS-based notebooks by putting hardware under the control of system software.

Because the U.S. PC market is so competitive, manufacturers are always looking for ways to differentiate their products without raising cost. One way to differentiate is by offering leading-edge technology before it becomes a commodity. Due to the market's characteristics, PnP ISA can be especially effective in the near future. This is particularly true when targeting the Fortune 1000 companies, which tend to purchase numerous portable computers.

Products are finally emerging that allow system manufacturers to add PnP support to their own products. Supported by standard software that's readily available from Intel, Microsoft, and numerous BIOS vendors, many notebook- and desktop-system OEMs are expected to rapidly adopt this technology.

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Add PnP Capability To An Existing Card

The PnP interface ASIC design can follow one of two paths.

BY BILL STANLEY
Adaptec Inc., 691 South Milpitas Blvd., Milpitas, CA 95035; (408) 945-8600.

The primary goal of the Plug and Play (PnP) specification is to make add-in boards and peripherals easier to install and configure. Needless to say, board vendors are looking to add this capability to their current and next-generation products.

The specification, developed by a coalition of more than 20 hardware and software companies, aims to simplify PC configuration for end users. Thus, PCs compatible with the Plug and Play BIOS specification will be able to seamlessly interact with the other two Plug and Play components—the operating system and I/O devices. Specifically, the PnP standard defines the hardware and software required to allow dynamic reconfiguration, while preventing system conflicts. Systems that are completely compatible will internally resolve all conflicts to guarantee boot-up every time an I/O device is added or eliminated.

Two varying design approaches can be applied when adding PnP capability to an existing card. The first is to redesign the ISA interface ASIC (if one exists). The second is to design an add-in PnP ASIC (front end) for use between the ISA bus and peripheral.

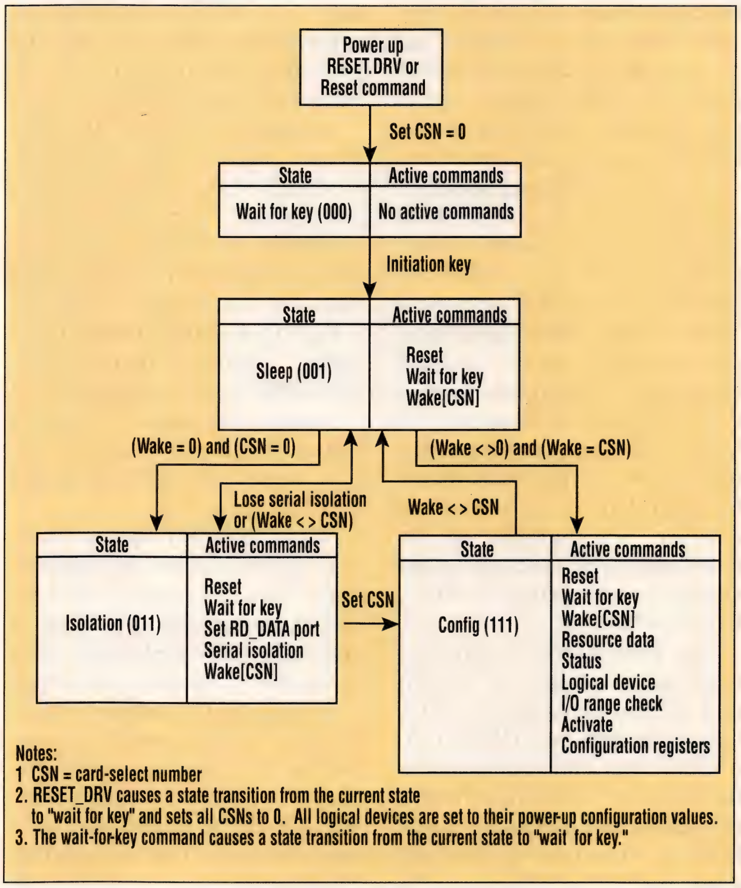
The first option typically produces a lower-cost design because it minimizes the parts count and uses existing hardware. However, if the PnP portion must be added to an existing ASIC, the time required to modify a complex IC may severely impact the design's time to market. Conversely, a carefully designed front-end PnP ASIC (option two) may hasten the product's design cycle. If the current design employs PLDs for the decode portion, it would be a good candidate for a front-end PnP ASIC. By creating a flexible design, the resulting ASIC can easily adapt to future products.

Regardless of which path the designer follows, some common functional blocks must be designed into the ASIC to maintain PnP compatibility. They include common signals, a PnP state machine, a PnP address-register select, variable read-data port (RDP), key detect, EEPROM control, arbitration logic, read-resource control, and a PnP register set.

Some other blocks may also be required, depending on the ISA card source requirement. These include variable memory and I/O decode, an interrupt-request multiplexer, a data-request and acknowledge multiplexer, and ISA bus access to the data stored in the EEPROM.

Before designing the individual blocks of the ASIC, some thought must be given to two common signals used throughout the device—Reset and Clock(s). The PnP ASIC needs a reset signal to initialize itself at power-up, and can generate a software-controlled reset to external circuits. If the ISA reset signal (pin B2) is used as a reset source, some analog or digital filtering must be employed be-

1. The four possible PnP state transitions are wait for key, sleep, isolation, and config (the state-machine codes are shown in parentheses). A reset forces all three of the state bits to 0.



Notes:
1 CSN = card-select number
2. RESET_DRV causes a state transition from the current state to "wait for key" and sets all CSNs to 0. All logical devices are set to their power-up configuration values.
3. The wait-for-key command causes a state transition from the current state to "wait for key."

cause of the noise.

In addition, the internal state machines and EEPROM shift register within the ASIC will need a clock source. Since the maximum clock rate for the serial EEPROM is 1 MHz, the 14.138-MHz oscillator clock on the ISA bus can be divided by 16 to provide a reasonable shift speed.

A good starting point in the design of a PnP interface ASIC is with the internal state machine. It tracks the PnP state as the host communicates with PnP devices. The card can be found in one of four possible states: wait for key, sleep, isolation, or configuration *(Fig. 1)*. While the four states could be represented with a two-bit state machine, a three-bit device simplifies coding and asynchronous state changes.

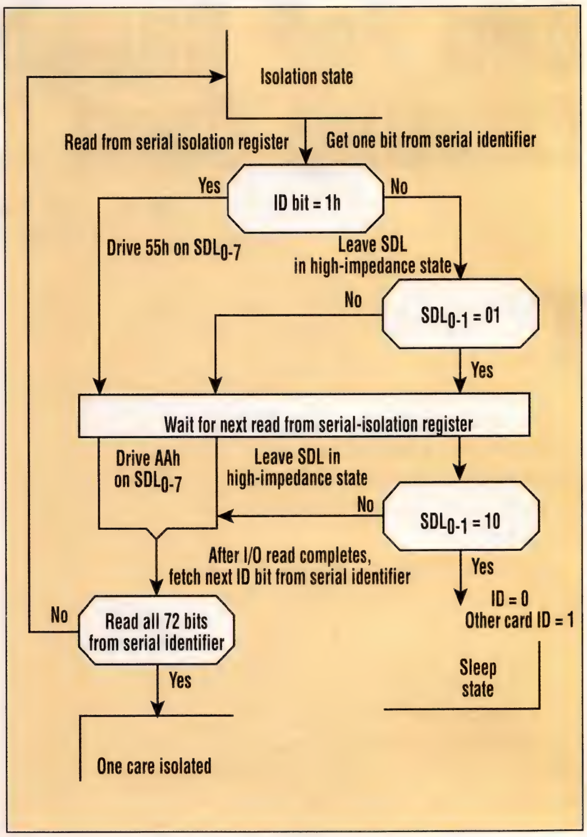
In the state machine, bit 0 (the LSB) is set when a valid key sequence is detected by the key-detect logic. It remains set until the next reset event occurs (hardware, software, or wait-for-key command). Bit 1 is pulled high by any wake[CSN] command. Bit 2 (the MSB) is set by one of two possible conditions: a wake[CSN] command, if wake $\neq 0$ and wake = CSN; or a set[CSN] command while the current state is in the "isolation" mode. Both bits 1 and 2 are cleared either by a wait-for-key command or the LOSE_ARB signal from the arbitration block. Because the timing of these state changes is somewhat asynchronous, the actual state output signals from the state-machine block should be generated by a synchronous decoder. For example, the decoder could be clocked by the system crystal (about 8 MHz) from the ISA bus.

The PnP interface only allocates one 8-bit port for reading and one for writing—the RDP and write-data port (WDP). As a result, there must be an internal means of selecting which of the many PnP registers is read from or written to. A write-address port (WAP) fixed at I/O-port address 279h usually handles this task. To access any PnP register, its address must first be written to the WAP. Then, any read to the RDP or write to the WDP will access the correct PnP register. The PnP state determines which registers can be accessed.

The RDP is relocatable within the 200h to 3FFh range of I/O space. This is the only read register available for PnP operation. Because the single-byte register is relocatable, the decoder must compare ISA address bits 1 through 11 to the contents of an 8-byte register and four fixed-value bits. Bits 0 through 7 compare with ISA-bus address bits 2 through 9. ISA address bits 0 and 1 must be "one" and bits 10 and 11 must be "zero." Since the RDP is located above address 200h, bit 7 of the RDP is used as both a decode compare bit and as a decoder enable. If bit 7 is zero, the decoder will be disabled. Because a Reset will clear all of the bits, accidental decoding of the RDP prior to its address being initialized will be prevented (this register is decoded as PnP register 00h).

A sample design of the Key Detect block, called the linear-feedback shift register (LFSR), is depicted in appendix B of the published PnP ISA specification. Designers must add three features: the ability to preset the LFSR to a value of 6Ah upon Reset; a detector that matches the LFSR to the write data; and a counter that detects 32 correct writes. The detection of 32 correct writes sets the LSB of the PnP state machine.

The EEPROM control block isn't defined in the PnP specification and will probably present the most challenging portion of the design. The EEPROM must retain the ID of the PnP device (8 bytes) and the resource information, which varies in size (about 75 bytes per logical device). In addition, this EEPROM can be loaded with data to initialize the PnP chip and replace jumpers.

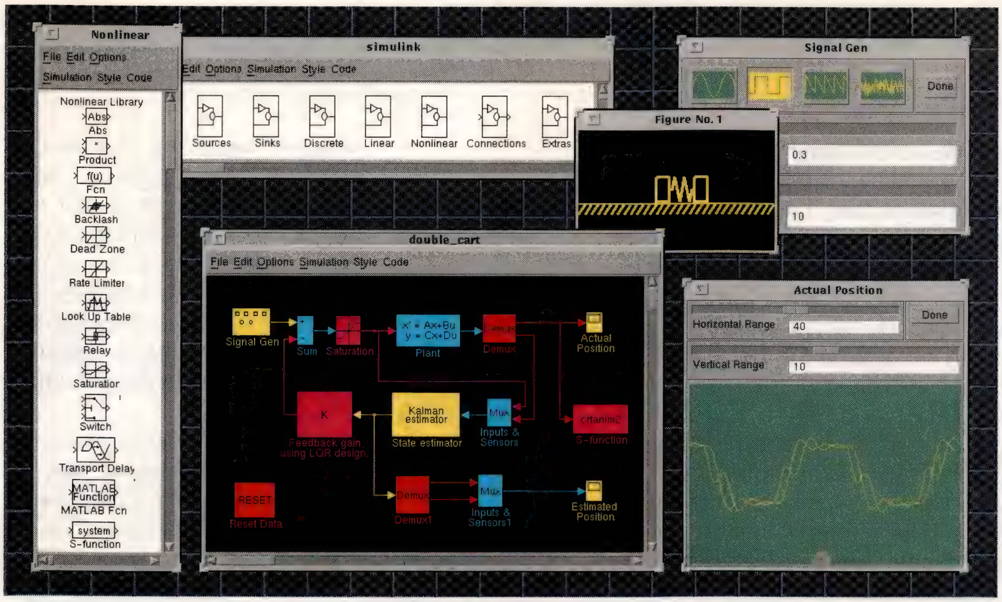

Isolation state
Read from serial isolation register
Get one bit from serial identifier
Yes
ID bit = 1h
No
Drive 55h on SDL_{0-7}
Leave SDL in high-impedance state
No
SDL_{0-1} = 01
Yes
Wait for next read from serial-isolation register
Drive AAh on SDL_{0-7}
Leave SDL in high-impedance state
No
SDL_{0-1} = 10
After I/O read completes, fetch next ID bit from serial identifier
Yes
No
Read all 72 bits from serial identifier
ID = 0
Other card ID = 1
Sleep state
Yes
One care isolated

2. The algorithm that isolates each PnP card uses the signals on the ISA bus and requires lock-step operation between the PnP hardware and isolation software.

In a design that was actually built, a 93C56 three-wire serial EEPROM was employed. At reset, 15 bytes of jumper simulation and configuration data was automatically loaded into the ASIC. Once the ASIC entered the Isolation state, the ID was read from the EEPROM to be used for arbitration. Finally, in the Config state, the resource data was read from the EEPROM and made available to the host. Four separate state machines supplied flexible access to the EEPROM.

In the example, the first state machine took a 9-bit address and generated all of the serial signals needed to read from the EEPROM. It then generated the read op code, added the address, and shifted the 8 read-data bits into a serial-to-parallel converter. "Reading" and "Done" status bits update other state machines of the read progress.

At reset, the second state machine reads the 15 initial data load (IDL) bytes. The IDL machine generates the EEPROM address for the data, starts the



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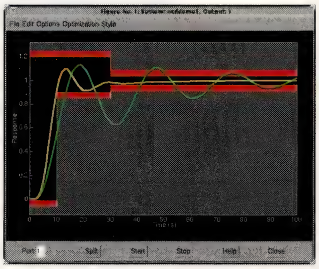

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read state machine, and writes the bytes into the correct internal registers. When finished, an IDL_Complete bit permits the next state machine to start.

The third state machine starts when IDL_Complete is true and the PnP stage changes to Isolation. This state machine uses a 4-bit pointer to read the ID data from the EEPROM to the arbitration block. The final state machine sends the data sequentially from the EEPROM to the read-resource data register while in the Config state.

The arbitration logic is responsible for implementing the isolation-protocol portion of the PnP specification. The checksum for the 8-byte ID field can either be generated on the fly or hard-coded into the EEPROM's ninth byte. Because the ID is read-only (factory-written) and takes no additional hardware, the ASIC uses the hard-coded means to generate the checksum. The arbitration logic consists of four hardware components: a 144-state (72-by-2) counter; a three-state driver on the ISA data-bus bits (0 to 7) that can drive either 55h or AAh; a detector for either a 01 or 10 (binary) pattern on ISA data bits 0 and 1; and a small state machine to implement the PnP card-isolation algorithm *(Fig. 2)*.

The resource-data reading is handled by the aforementioned state-machine method. Note how the "done" bit of the EEPROM read state machine supplies the status bit needed for register 05h. The design should employ just one pointer for both the arbitration ID and the resource data, which is cleared to 00h by any Wake[CSN] command or reset.

The various PnP registers are implemented as needed and are selected based on the decode process. The register read should be designed so that any read to a nonexistent register returns a value of zero. One exception to this rule involves the DMA channel-select registers at 74h and 75h: If these registers aren't used, a read should return a value of 04h.

(Note: The current version of the PnP specification can be downloaded from Compuserve by typing "Go Plugplay.")

The arbitration logic is responsible for implementing the isolation-protocol portion of the PnP specification.

Bill Stanley, a senior development engineer at Adaptec, received BSEE, MSEE, and MSCIS degrees from San Jose State University, San Jose, Calif.

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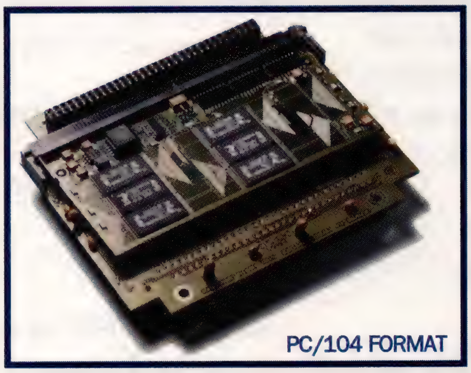
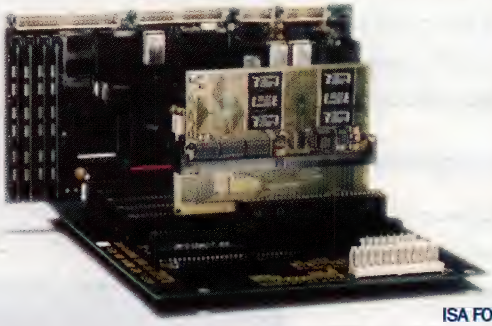
25 MByte FlasHD Memory Module


PC/104 FORMAT

"The FlasHD card allows a system to boot without mechanical drives, execute applications and write up to 25MBytes of non-volatile storage."

EMBEDDED-PC PC/104 MODULES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- ▶ Hard Drive replacement; supports M-Systems
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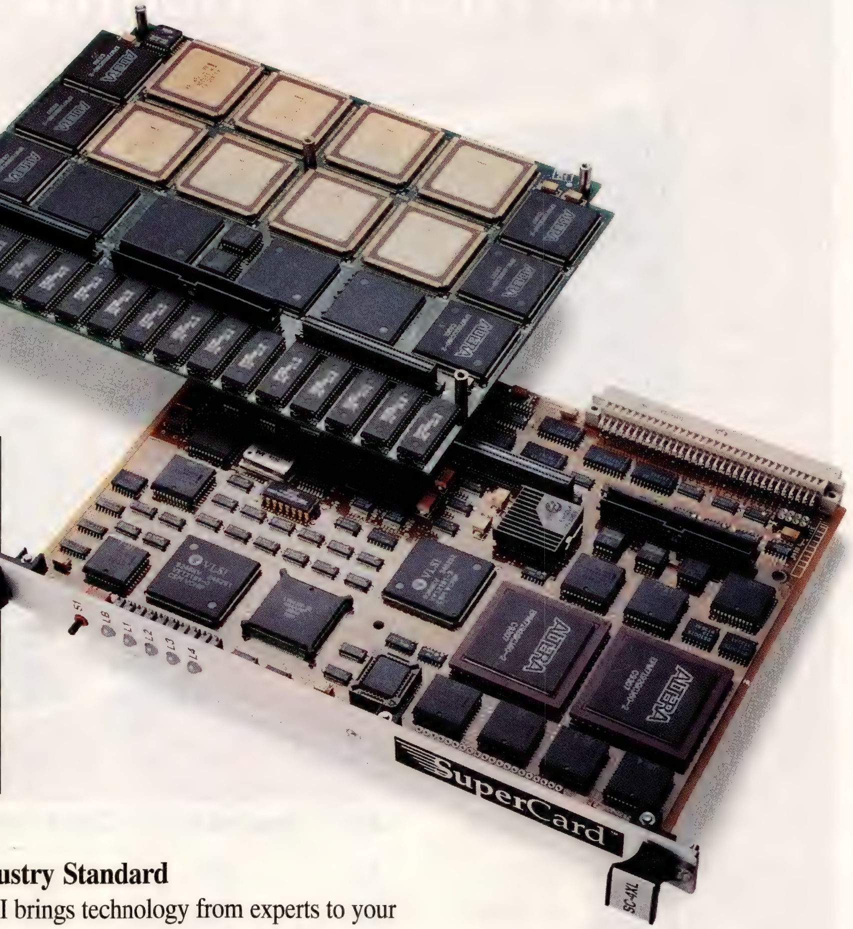
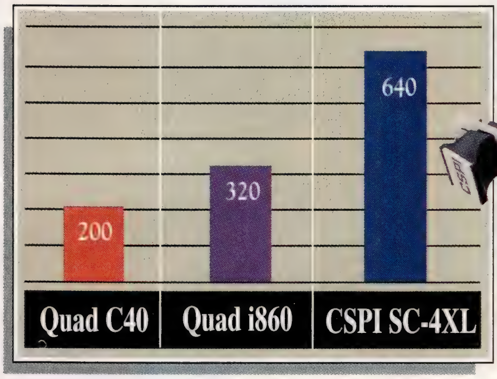
The Logical Choice for Multiprocessor Power – SuperCard-4XL Architecture



Million floating point operations per second on 6U VME board



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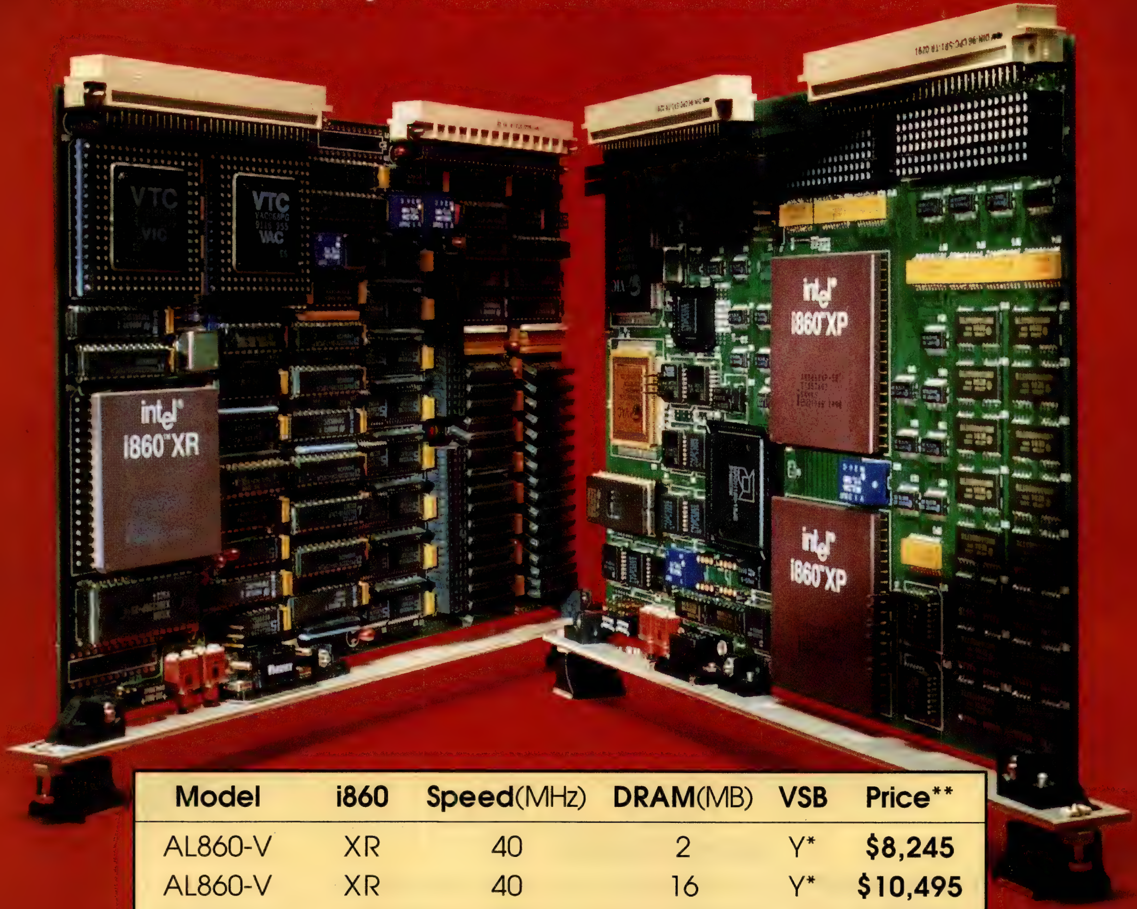
READER SERVICE 85

ALACRON i860 VME

The Price / Performance Leader



Model	i860	Speed(MHz)	DRAM(MB)	VSB	Price**
AL860-V	XR	40	2	Y*	**$8,245**
AL860-V	XR	40	16	Y*	**$10,495**
FT*200*/1-V	XP	50	16	Y*	**$12,290**
FT*200*/2-V	dualXP	50	16	Y*	**$15,290**

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ALACRON

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All product information is accurate as of January 1993. *VSB daughter board option included in price.
**Suggested list price effective January 1993. Trademarks are property of their respective owners.

READER SERVICE 80

SYSTEM DESIGN NEWS

The anticipated growth in the personal-digital-assistant (PDA) market as well as proliferating digital appliances, from television remote controls to mice to who-knows-what, is creating an infrared (IR) communications nightmare. A recently established association, the Infrared Data Association (IrDA), Walnut Creek, Calif., hopes to prevent a Tower of Babel by trying to standardize the IR communications protocol and pulse structure used by PDAs and other wireless devices to exchange data. With the membership consisting of more than 50 computer and telecommunications hardware and software suppliers, the organization is striving to make interoperability a reality between the multitude of portable devices with IR serial I/O ports.

At last month's IrDA standards meeting, close to 60 representatives met to iron out details of the first-generation standard. The basic goal of the standard is to provide an outline that defines a serial data link that can support data rates of up to 115.2 kbits/s. To do that, the committee has two major sub-efforts going on: defining the protocol employed to transfer the data, and defining the physical layer (including the pulse duration) for the actual data transfer and communications.

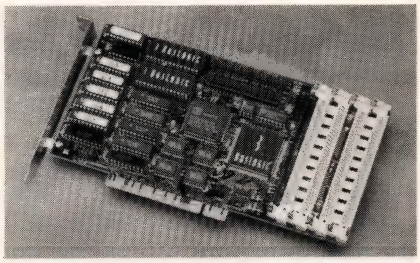
Final voting on the standard won't take place until mid-February, with a target release date of mid-March at the CeBIT conference in Hannover, Germany. However, many of the details are fairly firm for the standard's first iteration. For instance, the protocol used for data transfer will be HDLC-SIR (high-level data-link control-serial IR), which is employed in Hewlett-Packard Co.'s (Palo Alto, Calif.) Omnibook and pocket-sized computers. The protocol allows for a 32-bit global address, a 7-bit device address (up to 128 devices in an optical cone), and master-slave operation. It also permits address resolution in situations where two or more devices have the same 32-bit global address. The data-link layer being defined by the committee includes various issues, such as media-access control rules, addressing, device discovery, negotiation, and HDLC information exchange.

On the physical side, the committee is examining the pulse structure, which also is based on HP's serial IR scheme. The basic definition is that a logic "0" will be represented by a pulse with a width that's either fixed at 1.6 μs, or is variable and can be as short as 1.6 μs or as long as 3/16th the bit period. The committee voted last month and selected the second option, which permits a variable or fixed-width pulse. The variable was preferred because the fixed version is just a specific subset, so the variable option includes it anyway. Furthermore, the variable-width option is expected to be more adaptable to lower-speed systems that may not be able to generate the narrow, 1.6-μs pulses.

In addition, maximum and minimum transmit power levels, maximum and minimum receiver sensitivity, and the angular spread of the infrared has been agreed upon and documented. To supplement these specifications, a detailed physical-layer test definition document is being prepared. These specifications are for a distance of 1 meter, but allow for a 3-meter option.

As part of the test specification, methods are being developed to ensure that all devices are tested to the same requirements. Furthermore, the committee is trying to define an additional layer of interface software that will reside between the hardware and the application packages. The subcommittees are also pushing to come up with an IrDA logo that can be used to identify the organization and devices that are "IrDA compatible," and a set of rules to define who can use the logo and what the logo means when it's displayed on a device. For IrDA information, contact John LaRoche at (510) 943-6546; or by E-mail: jlaroche@netcom.com. For technical questions, contact Dr. Steven Harris, Crystal Semiconductor at (512) 442-7555, ext. 253; or by E-mail: snh@crystal.cirrus.com.

▼ IDE CACHE CONTROLLERS EXPLOIT LOCAL BUSES



A trio of high-performance IDE cache-controller kits increase I/O performance for PCI-, VL-Bus-, and ISA-based platforms. By employing the kits, bottlenecks between slow I/O bus interfaces and IDE disk drives are reduced. Included are a cache-controller board with a built-in configuration utility, cables, and documentation. The two local-bus units also come with 32-bit drivers for enhanced support in MS-DOS/Windows, Netware, OS/2, and Unix. The configuration utility simplifies installation and allows for drive customization.

The controllers combine expandable SIMMs with optimized caching algorithms to increase the throughput of data from the IDE subsystem to the host microprocessor. They also supply disk-mirroring and linking capabilities. In addition, the controllers increase the number of drives, four hard disks and two floppies, that can be connected to the system. Each hard-disk drive can have a maximum capacity of 4 Gbytes. Cache memory on the kits ranges from 515 kbytes to 16 Mbytes. Different capacity SIMMs can be mixed and matched on the same board.

The PCI and VL-Bus kits offer data rates of 5 Mbytes/s on the IDE subsystem side and 20 Mbytes/s on the system-bus side. Average seek time is less than 0.3 ms. The PCI controller offers complete plug-and-play compatibility. The maximum transfer rate on the ISA board is 5 Mbytes/s in either direction.

All three kits are available now. The KT-410A for the VL-Bus costs $175; the KT-910A PCI unit sells for $225; and the KT-510A for the ISA bus is priced at $105.

BusLogic Inc.
4151 Burton Dr.
Santa Clara, CA 95054
(408) 492-9090
▶ CIRCLE 625

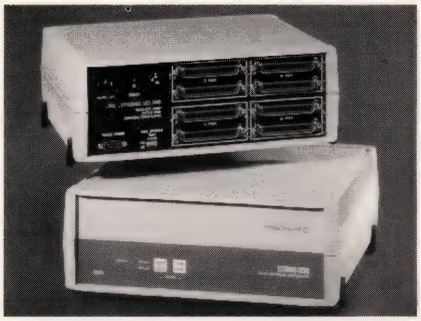
▼ BUILD A MULTIMEDIA BOARD FOR UNDER $100

Multimedia products, with graphics resolutions up to 1280 by 1024 pixels, can be brought to market with a bill-of-materials cost of under $100. The Bt895 video controller, which becomes the heart of the design, performs all of the system interface and control functions, such as simultaneous display and capture to disk, accelerated playback, and frame-buffer memory control. To reduce the time to market, a developer's kit is available. The kit includes everything needed to build a complete multimedia board, as well as VHDL synthesis source for the Bt895 and source files for the audio, video, and graphics functions. The kit sells for $2900. The 160-pin Bt895 goes for $16 each in quantities of 10,000.

Brooktree Corp.
9868 Scranton Rd.
San Diego, CA 92121
(619) 452-7580
▶ **CIRCLE 626**

▼ SWITCH TO REMOTE SCSI DEVICES

Both local and remote switching of SCSI systems and peripherals can be done using the SCSI Switch, model ACI-2012. Compatible with fast SCSI, the device allows peripherals on independent SCSI buses to be connected and exchanged electronically without reconfiguring cables or bus terminators. Installation is easy. Daisy-chained connectors on the rear panel attach to each SCSI device. Cable distances of up to 40 ft. can be accommodated. Switch selection is controlled by the front panel or a remote RS-232 connection. The front-panel indicators identify selected SCSI ports and bus activity. The SCSI Switch conforms to ANSI X3.131 and X3T9.2 specifications for single-ended devices. Three different versions are available. The 2012A comes with 50-pin Centronics connectors and sells for $1375. The 2012B has 50-pin flat ribbon connectors and costs $1325. The 2012C, priced at $1425, offers 50-pin high-density connectors. All units come with externally-selectable 110/220-V ac input.



Applied Concepts Inc.
9130 S.W. Pioneer Ct.
Wilsonville, OR 97070
(503) 685-9300
▶ **CIRCLE 627**

▼ 4.1-LB. COMPUTER BOASTS COLOR DISPLAY

Color displays on notebook-size computers are becoming the norm, and the Portégé T3400CT is no exception. Built with a TFT-LCD active-matrix display, the 4.4-lb. computer measures 7.9 by 9.9 by 1.8 in. The system is built with a 33-MHz 486SL microprocessor that operates from a 3.3-V supply. A lithium-ion battery supplies 4 to 8 hours of operating life. Expansion is achieved through a Type 2 PCMCIA slot. Here, users can plug in various options, such as memory or communication devices. The AccPoint built-in isometric pointing device is placed between the G, H, and B keys (similar to IBM's ThinkPad). Click and drag buttons sit at the front of the recessed keyboard. A VL-Bus local-bus graphics accelerator speeds up the images displayed on the color panel. The base unit contains 4 Mbytes of RAM (expandable to 20 Mbytes). Prices start at $3999. A monochrome model is available.

Toshiba America Inc.
P.O. Box 19724
Irvine, CA 92713
(800) 334-3445
▶ **CIRCLE 628**

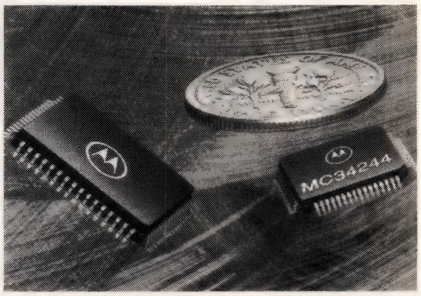
▼ HIGH-PERFORMANCE CHIP SET SUPPORTS MULTIMEDIA

Designed for data and fax modems as well as voice and business audio functions, the RCV144ACi-BA offers a low-cost, high-performance multimedia solution. The chip set, which handles 14.4-kbit/s transmission speeds, also supports 2-, 3-, and 4-bit voice compression-decompression at 7200 Hz and 8- and 16-bit audio record and playback at 7.2 or 11.025 kHz. The microcontroller firmware performs extended AT commands, supplying V.42/MNP 2-4 error correction, V.42bis/MNP5 data compression, and other relevant standards. The chip set consists of a 68-pin PLCC data pump and an 84-pin PLCC microcontroller. Available now, the set sells for $77 in quantities of 10,000.

Rockwell International Corp.
4311 Jamboree Rd., P.O. Box C
Newport Beach, CA 92658
(800) 436-9988
▶ **CIRCLE 629**

▼ READ-CHANNEL IC FITS IN TINY PACKAGE

Supplying all of the required functionality for the read-write channel in a constant-density hard-disk drive, the MC34244 read-channel IC can handle up to 48 Mbits/s. The device integrates automatic gain control, an active filter, a pulse detector, a data synchronizer, a frequency synthesizer, and a servo demodulator in a 64-pin, 10-by-10-mm TQFP package. Power-management functions combined with a 2.7-V supply voltage make the part suitable for portable applications. In quantities of 10,000, prices for the MC34244 read-channel circuit start at $18.50.



Motorola Inc.
Bipolar Marketing MD EL340
2100 E. Elliot Rd.
Tempe, AZ 85284
(602) 897-3615
▶ **CIRCLE 630**

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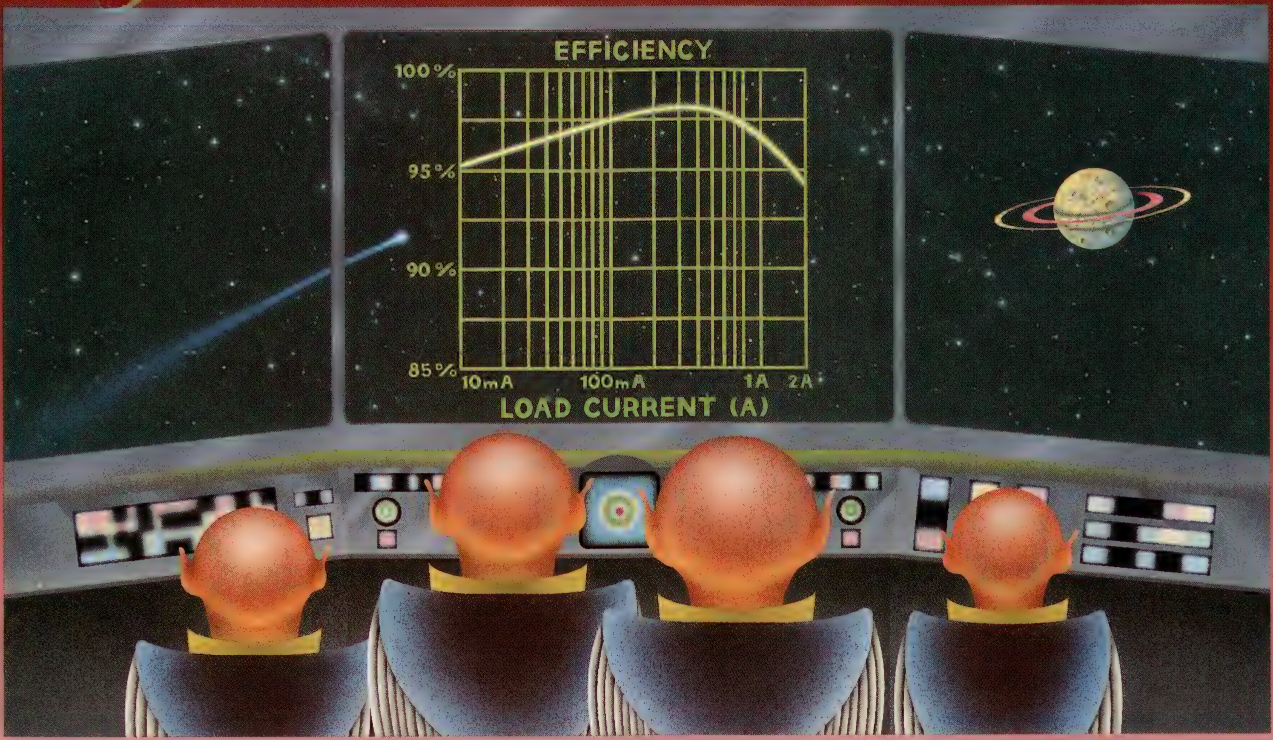

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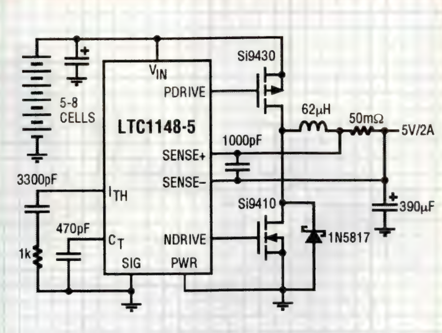
The LTC1149 extends synchronous switching with Burst Mode™ operation to input voltages as high as 48V. This makes it ideal for the high voltage AC adapters often used with 8-12 cell battery systems. Both the LTC1148 and LTC1149 feature soft-start, short circuit protection, and micropower shutdown.

LTC1148 and LTC1149 output options include adjustable, fixed 3.3V, and fixed 5V versions, and both are available in plastic DIP or SOIC (narrow) packages. Pricing starts at $4.34 in 1000 piece quantities for the LTC1148CS-5.



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READER SERVICE 167

▼ PORTABLE PC HOUSES PENTIUM PROCESSOR

Intel's latest microprocessor, the Pentium, is quickly becoming popular on the desktop. Now, thanks to the PAC-586, the high-powered processor is available in a portable model as well. The PAC-586 delivers 47 MIPS, out-pacing a similarly configured 66-MHz 486DX2 system by about 150%. The unit employs a liquid-cooling technique to take care of the heat problem sometimes found in the Pentium processor. Five full-length add-in board slots, three VL-Bus local-bus slots, three disk-drive bays, and a 275-W power supply are included. The TFT color display features 185,000 colors in a 640-by-480-pixel resolution. There's also a touch-screen option. Available now with 60- or 66-MHz Pentium processors, prices start at about $6000.

Dolch Computer Systems
372 Turquoise St.
Milpitas, CA 95035
(408) 957-6575
▶CIRCLE 631

▼ MODEM SENDS DATA AT 230.4 KBITS/S

Using data compression, the Optima 288 V.FC + Fax modem can send data at a rate of 230,400 bits/s. Standards supported by the external device include V.Fast, V.42bis, V.42, and Group 3 fax. In addition, it's backward-compatible with older industry standards. The modem is accompanied by Windows-based software for data and fax communications. The Optima 288 V.FC + Fax modem sells for $579. A 16-bit serial card with either one or two ports is necessary to achieve the 230.4-kbit/s data rate. It costs $99.

Hayes Microcomputer Products
P.O. Box 105203
Atlanta, GA 30348
(404) 840-9200
▶CIRCLE 632

▼ 2.5-IN. DISK DRIVES EMPLOY MR HEADS

A family of 2.5-in. hard-disk drives give notebook systems equal storage capacity to their desktop counterparts. The DHAA and DHAS drives hold 270, 405, and 540 Mbytes using either an AT (DHAA) or SCSI (DHAS) interface. Because the drives' high capacity comes from a proprietary magneto-resistive (MR) head technology, which pushes the areal density to 493 Mbits/in.^{2}, up to 270 Mbytes can fit on a platter. Using the AT interface, the transfer rate is 8 Mbytes/s. The fast SCSI adapter handles 10 Mbytes/s. In addition, an rpm of 3800 results in a 14-ms average seek time.

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▶CIRCLE 633

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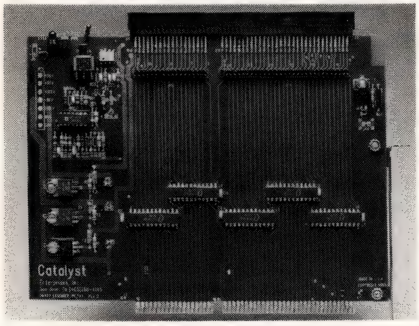
▼ EXTENDER BOARD PERMITS HOT SWAPPING

Compatible with the ISA bus, the Smart Extender PC/AT board makes it possible to hot swap a board-under-test without powering down the system or rebooting the system software. That's because all signals and power voltages are isolated. Voltages are ramped up and down to eliminate spikes. The board covers an entire address range and supports DMA operation without any software or switch setting. For debugging purposes, all bus signals are brought out to standard post terminals at the top of the board. The Smart Extender sells for $295.



Catalyst Enterprises Inc.
1439 Torrington Ct.
San Jose, CA 95120
(408) 268-4145
▶ **CIRCLE 634**

▼ DISPLAY PANEL CONNECTS TO PLC

The L70 smart display panel combines a message-display unit (MDU) and a counter-timer access module. The device is designed for operator-interface or control-panel applications. It can be programmed from a PC, and includes such features as a real-time clock and calendar, access to programmable-logic-controller (PLC) data registers, password protection, and a NEMA rating. The MDU offers two 16-character lines and seven key switches with LED indicators.

Logical Products Inc.
1486 St. Paul Ave.
Gurnee, IL 60031
(708) 336-6160
▶ **CIRCLE 635**

▼ TV INTERFACE BOARD PUTS VIDEO ON A PC

Users can capture, freeze, store, manipulate, and export fully-scalable digital video images by employing the 16-bit Video Galaxy TV-video interface card. As a result, video segments can be clipped from a television, VCR, camcorder, or laser-disk player.

The board supplies real-time control of hue, saturation, brightness, and contrast levels through software. Four audio software-controlled sources handle the volume, bass treble, and balance. An intuitive graphical user interface helps users get up and running quickly. The Video Galaxy board, which sells for under $300, is compatible with all major video standards, including NTSC. An upgrade module lets the board read Teletext.

Aztech Labs Inc.
46707 Fremont Blvd.
Fremont, CA 94538
(510) 623-8988
▶ **CIRCLE 636**

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READER SERVICE 111

SYSTEM DESIGN PRODUCTS

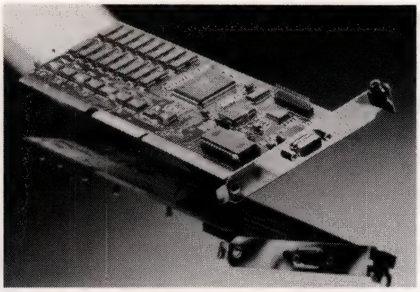
▼ TRANSPUTER BOARD SPEEDS APPLICATIONS

Using the Ultra/XL parallel-processing pc board, OEMs and systems integrators will be able to accelerate their existing software. The board features a 16-bit interface that can handle up to 10 standardized transputer compute modules (TRAMs), thus providing a scalable development environment. As more performance is needed, more TRAMs can be added. Flexibility is increased by using a software-programmable 64-by-64-point crossbar. The crossbar connects the TRAMs and supplies an interface to other external transputer boards and systems. The Ultra/XL comes with a DOS driver, debugging tools, libraries, utilities, operating environments, and configuration and diagnostic software, including ANSI C, C++, Occam, and other compilers. Support for Novell LANs will be available shortly. Prices start at $1195.

Alta Technology
9500 South 500 West, Suite 212
Sandy, UT 84070
(801) 562-1010
▶CIRCLE 637

▼ VIDEO ACCELERATOR BASED ON THE W32i

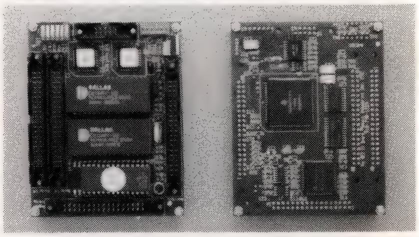
The Phantom 32i is a 32-bit Windows and CAD interleaving graphics accelerator board based on the Tseng Labs W32i chip. The DRAM-based board takes advantage of the 32-bit VL-Bus local-bus interface. Two versions are available: The 8900VL-20 holds 2 Mbytes of DRAM, while the 8900VL-10 comes with 1 Mbyte. The maximum resolution supported is 1280 by 1024 pixels. A proprietary FlickerFree technology eliminates screen flash and flicker. Drivers are included for Windows, OS/2, AutoCAD, and other popular applications. The 8900VL-20 sells for $349, while the 8900VL-10 costs $269. The 1-Mbyte board can be upgraded to 2 Mbytes for $119.



Genoa Systems Corp.
75 East Trimble Rd.
San Jose, CA 95131
(408) 432-9090
▶CIRCLE 638

▼ FLOATING-POINT BOARD SUITS EMBEDDED APPS

The QED board supplies fast floating-point computation and instrument control in a package that's small enough to integrate into most embedded designs. The on-board, high-level language facilitates programming through any PC or terminal. Up to 384 kbytes of memory include battery-backed write-protectable RAM, which eliminates the need for PROM burning. The battery-operable, surface-mounted board supplies up to 60 I/O lines.



Mosaic Industries Inc.
5437 Central Ave., Suite 1
Newark, CA 94560
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▶CIRCLE 639

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The MR-CPU440 processor board can now handle a temperature range that extends from –40 to +85°C. The rugged board employs independent modules for the processor, memory, and I/O interfaces, connected by a high-performance DMA bus. The 100-Mbyte/s DMA channel links the 68040 CPU, a 68302 communication processor, and a 16-Mbyte memory to the VME64 interface. Both block and DMA transfers are supported, yielding a VMEbus transfer rate of 70 Mbytes/s. An additional 16 Mbytes of DRAM are available as a local resource to the main processor. Extensive operating-system support is available. Prices for the MR-CPU440 start at $7350.

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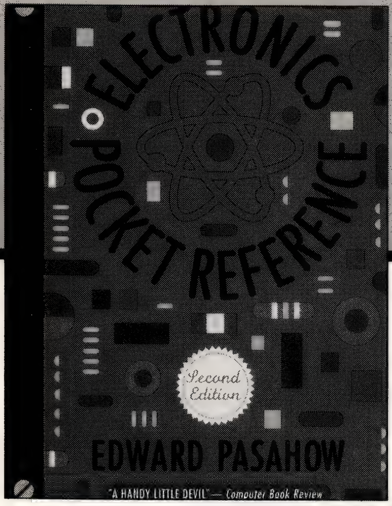
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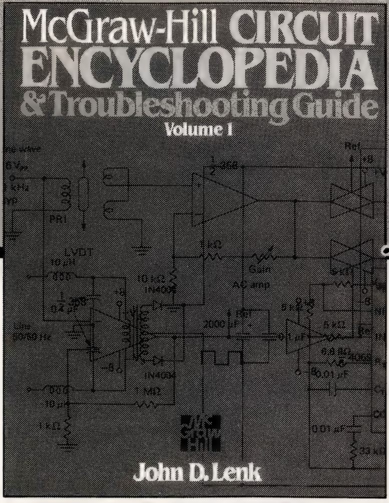

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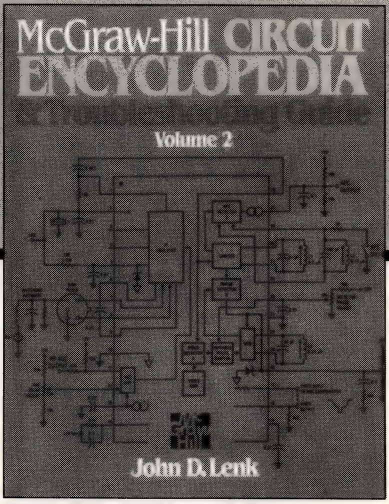

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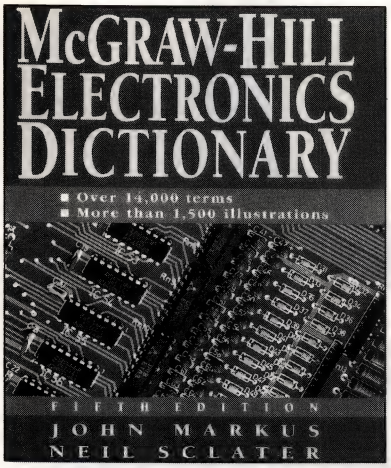
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A Short Quiz for America's Executives

1. **Would you like to help disadvantaged young people get an education—and a job?** ☐ YES ☐ NO

2. **Does your company have excess inventory, services or assets that could be used by colleges?** ☐ YES ☐ NO

3. **Could your company use an above cost tax deduction for qualified inventory donations?** ☐ YES ☐ NO

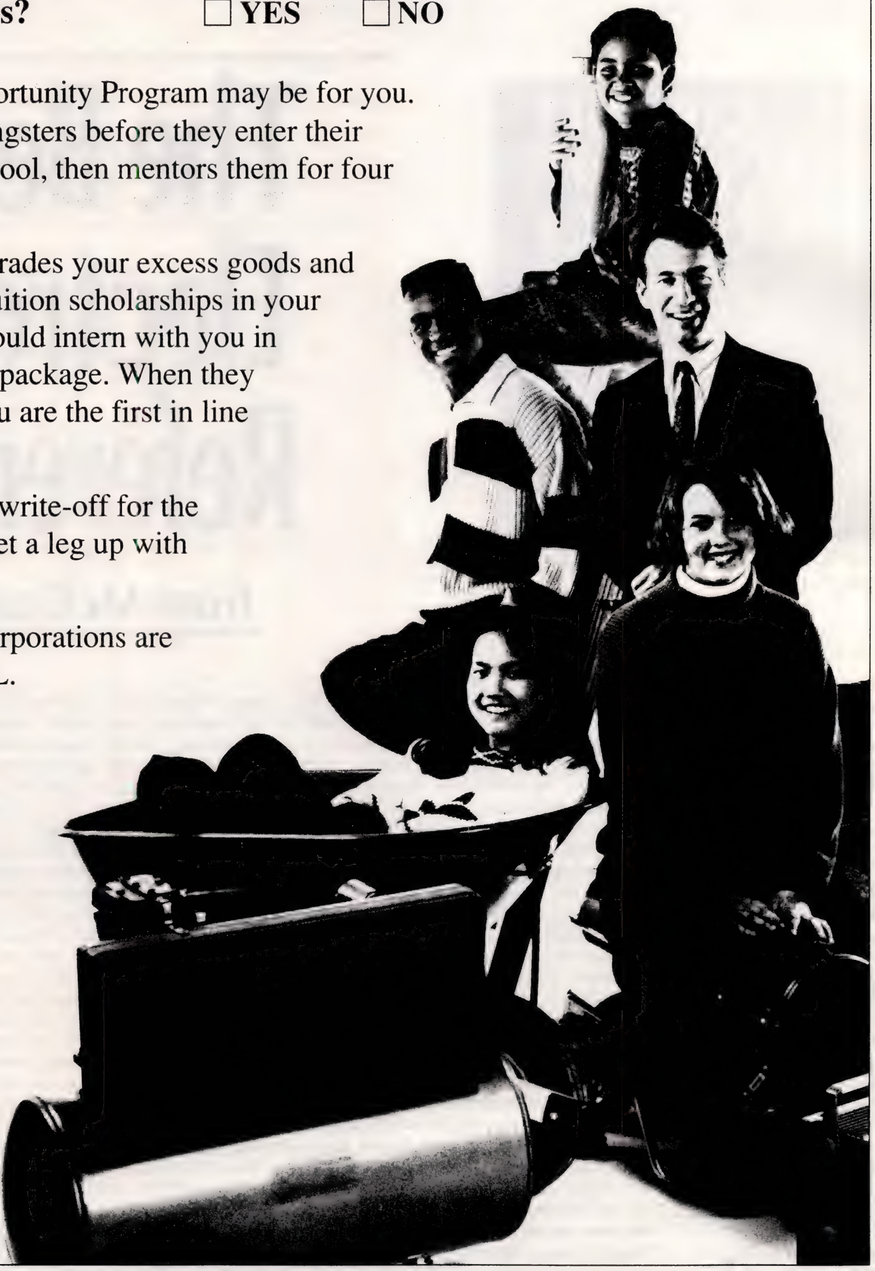
If so, EAL's College Opportunity Program may be for you. EAL targets talented youngsters before they enter their freshman year of high school, then mentors them for four years until they graduate.

How does it work? EAL trades your excess goods and services to a college for tuition scholarships in your name. And the students could intern with you in the summer as part of the package. When they graduate from college, you are the first in line to recruit them.

The result? You get a tax write-off for the donations. And the kids get a leg up with their education. Not bad!

Many of America's top corporations are already committed to EAL.

Why not join them?



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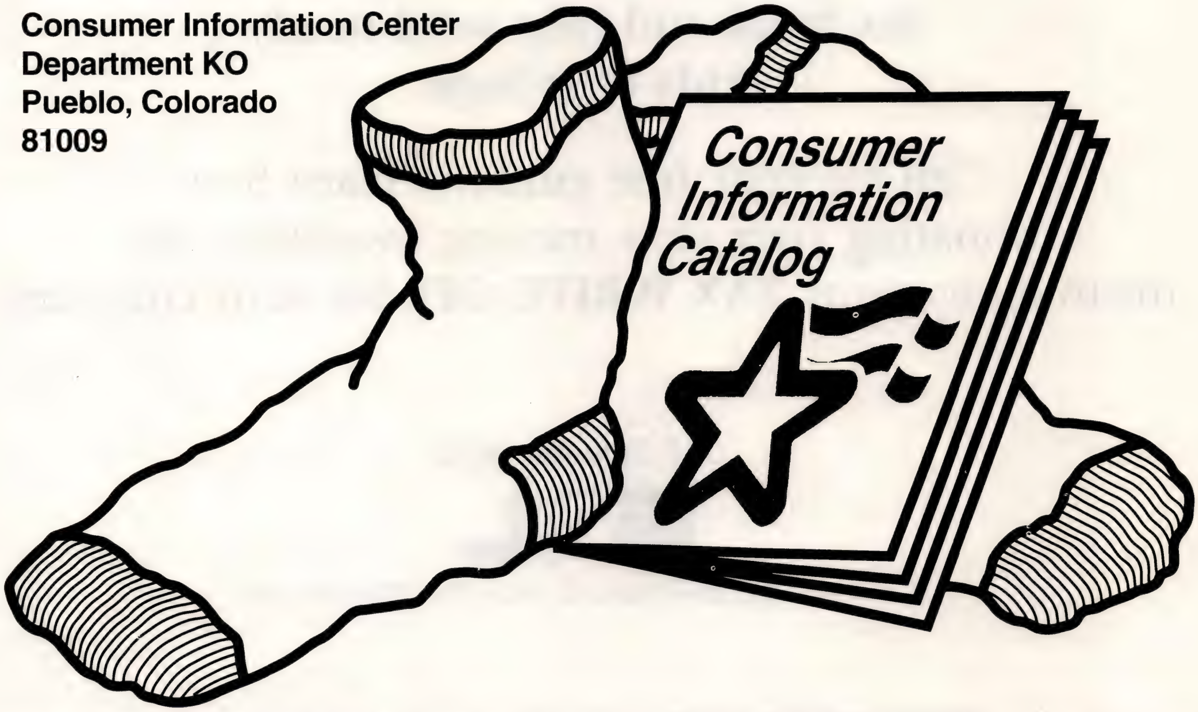

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PRODUCTS NEWSLETTER

COLOR PALETTE CHIP PACKS DACS AND CLOCKS

The GENDAC II single-chip video subsystem from Integrated Circuit Systems, Valley Forge, Pa., combines triple 8-bit video d-a converters, two programmable-frequency timing generators, and a color-palette memory on one chip. The CMOS color palette also has a 16-bit pixel-input port that supports 24-bit true color, 16- and 15-bit high color, and 8-bit pseudo-color applications. The RAM palette displays 256 colors selected from a possible 262,144—more colors are possible by using the chip's bypass mode. GENDAC II supports dot-clock speeds of up to 135 MHz, and can drive screens with up to 1280 by 1024 pixels at a refresh rate of 72 Hz. One of the two on-chip PLLs lets designers set any of eight video clock frequencies, six of which are user-programmable, while the other clock generator makes it possible for designers to select one of two programmable memory clocks. Anti-sparkle circuitry on the chip reduces image snowing and sparkling. In lots of 50,000 units, the 135-MHz chip sells for $9 apiece, while a slower version sells for $6.95 in similar quantities. Samples are available from stock. *DB* CIRCLE **661**

ANALOG DESIGN TOOLS DROP IN PRICE

Intergraph Corp., Huntsville, Ala., has repackaged and lowered the price on its analog design software for Intergraph and Sun workstations. The company dropped the price of its Apex analog-simulation engine from $15,000 to $10,000, and also repackaged its suite of analog analysis tools into three core products. The first, Analog Designer, provides the simulation control and graphical user interface for all of the company's analog and mixed signal tools. It costs $5000. Analog Engineer, which also costs $5000, provides a suite of tools for high-frequency and specialty applications. Key features are stability analysis, two-port analysis, filter design, and switched-mode power-supply design. The third package, Analog Model Library, contains Intergraph's general, special, and automotive libraries for $10,000 (reduced from $36,000). Models include digital logic, control engineering, and microwave components. Call (800) 345-4856. *LM* CIRCLE **662**

ADA TOOLKIT AIMS AT 68XXX

TartanWorks, Ada development tools for the Motorola 68xxx, integrates the VxWorks real-time operating system from Wind River Systems, Alameda, Calif., with the Tartan Ada Development System. As a result, developers can generate highly optimized code for real-time, embedded applications that run on commercial and military Motorola 68xxx boards. The cross-development system from Tartan, of Monroeville, Pa., includes an optimizing Ada compiler, multiuser Ada program librarian, an Ada runtime system integrated with the VxWorks OS, a function library, flexible linker, source and machine-level debugger, utilities, on-line help, and documentation. The system runs on Sun Sparc workstations. For more information, call (412) 856-3600. *SVT* CIRCLE **663**

LET HOST HANDLE PRINTER COMPUTATIONS

Using the WinStyler hardware-software combination, designers can envision 600-dot/in. laser printers, capable of running in a Windows or Macintosh environment, with street prices under $700. Moreover, the WinStyler, developed by Destiny Technology Corp., Santa Clara, Calif., can drastically improve the printer performance by shifting the computational burden. Because today's PCs are typically built with 33- or 66-MHz 486 microprocessors, the PC may be better suited than the printer itself to handle the printer's computations, such as imaging and rasterizing. Because the imaging is handled by the host, the problems associated with the various printer languages are reduced. Also, high-speed print jobs in both the Windows and Mac environments can be processed simultaneously by the WinStyler ASIC (called the QuickASIC). The graphical-device interface (GDI) software can rasterize and send 600-dot/in. images to the printer at speeds commonly associated with 300-dot/in. data, which is less complex. Because the bulk of processing is done on the host PC, the platform can perform previously unavailable functions. This is where the software comes in: Rather than have users rely on the simple interface offered by the printer, all communications between the user and printer can be handled through the PC, producing the GDI. Standalone printers based on the WinStyler technology should be available in the second or third quarter, followed by networked units in late 1994. Call Destiny at (408) 562-1000. *RN* CIRCLE **664**

Edited by Clifford Meth

"Increasing our ad budget was so successful, our agency recommended we cut it."

See what it's like to live 7 days without tranquilizers.
True, Columbus paid less than $945 getting to the Caribbean, but he had to take the Nina, the Pinta and the Santa Maria.
Sometimes you just gotta stop and smell the saltwater.
If you've never been early for anything in your life, it's probably because nobody made it worth your while.
With prices like these, you'd probably expect to row.
The last time the launching of a ship got this much attention it rained for 40 days and 40 nights.
The only thing standing between you and our cruise to Bermuda is $895 and an occasional pothole.
Once a year the swallows fly to Capistrano. The salmon swim to their spawning ground. And Floridians cruise to Bermuda.
It's like Monty Hall putting the big deal behind all three doors.
Sure you could crawl in a hole and hide. But wouldn't our bright spacious cabins be more comfortable?

Photo: Frank Moscati

Al Wallack, Sr. VP Marketing, Celebrity Cruises, after returning from having his hearing checked.

"A great time to introduce a new luxury cruise line. The economy was in a slump, and the competition was on the rise.

We told our new advertising agency we have to go in with all guns blazing. And gave them the extra money to do it.

They recommended a three phase campaign. Phase 1. Full page newspaper. One ad a week for 24 weeks and one-third pages in the travel section. Phase 2, radio. Then 3, television to sweep up one season and sow the seeds for the next.

To make a long story short, two-thirds into the newspaper phase, Celebrity's ships were just about full to the end of the season. With so little left to sell, we all agreed to hold the radio and TV and save the remainder of the budget.

In roughly two years Celebrity became the number one cruise line from New York to Bermuda.

We've just added another new luxury ship and we're anxious to fill it. So once again we've upped our budget. So far, our agency hasn't tried to talk us out of it."

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This advertisement prepared by Korey, Kay & Partners, New York.

WORKSTATIONS HARNESS 166- AND 200-MHZ ALPHA MICROPROCESSORS

The 166- and 200-MHz Alpha AXP microprocessors from Digital Equipment Corp. will appear in the Pantera I and II personal workstations from Carrera Computers. In addition, either are available in a motherboard-only configuration. The Pantera I holds the 166-MHz 21066 RISC processor on a baby AT-size motherboard in a standard desktop case. It comes with 16 Mbytes of RAM, 128 kbytes of secondary cache, a 250-Mbyte SCSI hard-disk drive, and an accelerated video adapter. The price for the system is $3995.

The Pantera I is built with 64-bit memory and processor buses and a 32-bit I/O bus, two 32-bit PCI slots, and three 16-bit ISA slots. Embedded controllers handle a parallel and two serial ports, SCSI, and Ethernet.

The Pantera II is based on the 200-MHz 21064 64-bit RISC CPU. The tower chassis holds 32 Mbytes of RAM, 1 Mbyte of secondary cache, a CD-ROM drive, a 500-Mbyte SCSI hard-disk drive, and accelerated video. The system configuration includes a 128-bit interleaved memory bus, a 64-bit processor bus, and a 32-bit I/O bus. The remaining features parallel those of the Pantera I. The Pantera II carries a $6995 price tag.

Carerra Computers Inc., *23181 Verdugo Dr., Suite 105A, Laguna Hills, CA 92653; (714) 707-5051.* **CIRCLE 680**

■ *RICHARD NASS*

WORKSTATIONS SUIT IMAGING AND MULTIMEDIA

Image-processing, multimedia, and video-capture and compression capabilities are built into the latest family of SparcStation platforms. The 10SX offers 24-bit color, 3D graphics, and hardware-accelerated video playback. Featuring a 535-Mbyte disk drive, 32 Mbytes of DRAM, and a 16-in. color monitor, it sells for $15,495. The model 10M starts at $17,095 and comes with all of the features of the 10SX. It also adds real-time video capture and compression as well as a video camera. The model M includes all of the hardware necessary to handle video conferencing over a standard network. Prices start at $4995. RN

Sun Microsystems Inc., 2550 Garcia Ave., Mountain View, CA 94043; (415) 960-1300. **CIRCLE 681**

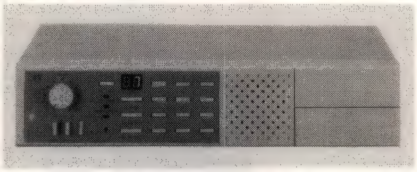
PORTABLE GPS FITS PCMCIA SLOT

Portable computer users can take advantage of a global positioning system (GPS) with the Mobile GPS, which is housed in a Type 2 PCMCIA card. Applications for such a device include field data collection, inventory control and personal navigation systems. Operating in an environment that ranges from 0 to +55°C, the satellite-based location system supports DOS, Windows, and PenPoint. The Mobile GPS consumes about 0.75 W in its active mode, and 25 mA in the sleep mode. A developer's software toolkit is available. RN

Trimble Navigation Inc., 645 North Mary Ave., P.O. Box 3642, Sunnyvale, CA 94088; (408) 481-8000. **CIRCLE 682**

ADD LIVE VIDEO IN A WINDOW

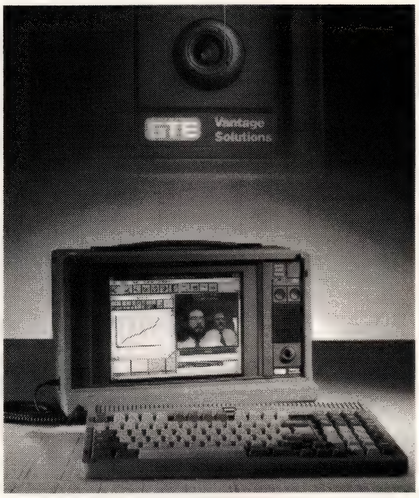
Live video windows can be integrated into a VGA computer display using the 722 PC Workmate. The window can sit in any portion of the display or can be used in a full screen. The 722 PC Workmate incorporates a full multiband VHF/UHF/CATV tuner that can receive up to 70 television channels. Also, the device has direct video inputs for a VCR, video disk, camcorder, or surveillance camera and a built-in speaker. Connected between the computer and the display, it merges the VGA signal and sends the combined signal to the display. With all the cables, the 722 PC Workmate sells for $525. Two different versions are available to support the NTSC or PAL standards. RN



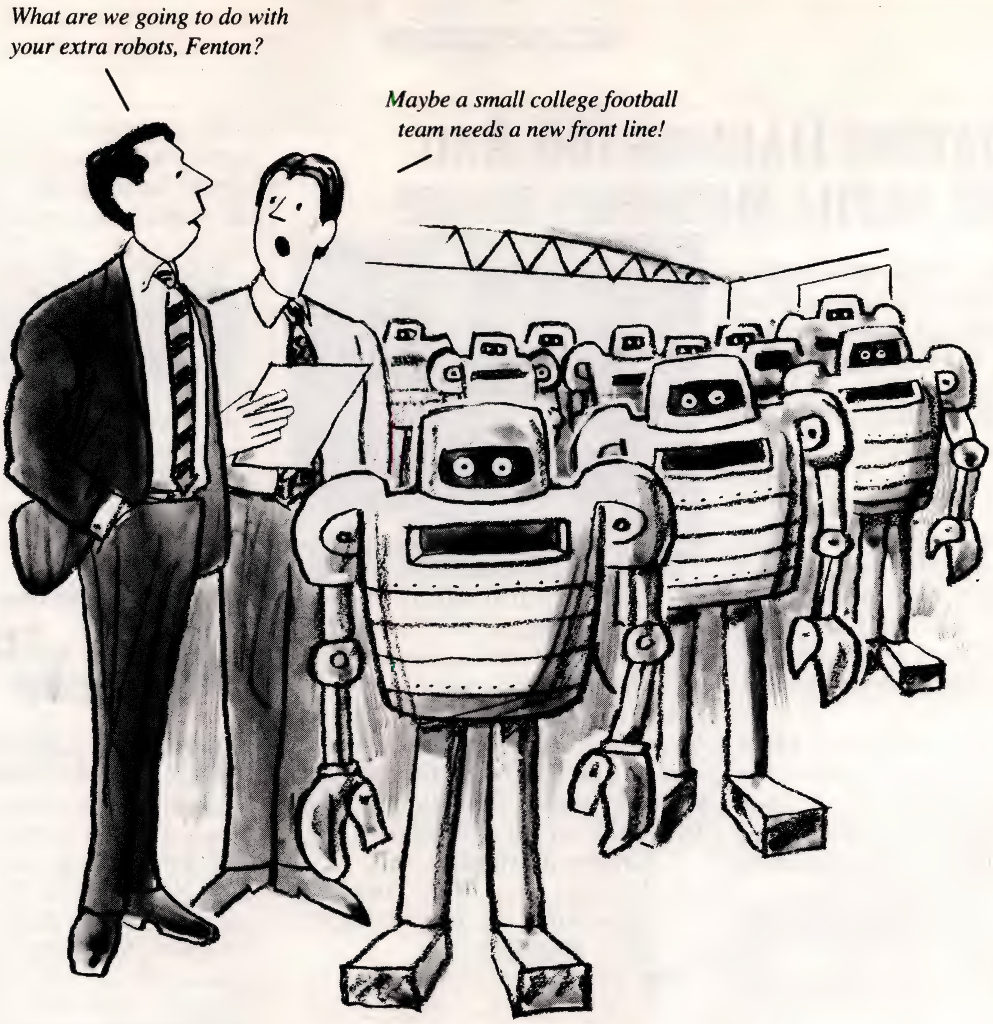
Telebyte Technology Inc., 270 E. Pulaski Rd., Greenlawn, NY 11740; (800) TELEBYT or (516) 423-3232. **CIRCLE 683**

TELECONFERENCE FROM A PORTABLE SYSTEM

A portable teleconferencing system is based on the work of two companies, Dolch Computer Systems and GTE Vantage Solutions. The 20-lb. package consists of the Desktop Video Teleconferencing System (DVTS) from GTE and the Portable Add-in Computer (PAC) from Dolch. Data is transmitted over ISDN digital telephone lines. The self-contained system contains an adjustable color video camera, a microphone, and a high-quality sound system. Video, voice, images, and documents can be sent with simultaneous annotation, all displayed under Windows. The systems will be available from Dolch. Prices should be under $20,000. RN



Dolch Computer Systems, 372 Turquoise St., Milpitas, CA 95035; (408) 957-6575. **CIRCLE 684**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Designed for use with large digitizer-based graphics systems, the Dakota series pedestals and workstations supply a stable and ergonomically correct work platform. The platform's computer shelf and accessory arms can be extended to hold a monitor or printer. The digitizing surface's angle and height can be adjusted and accommodates tablets up to 44 by 60 in.

The workstation requires an area of just 10.6 ft.^{2}. The Dakota series, built from heavy-duty construction material, is available immediately from stock. RN

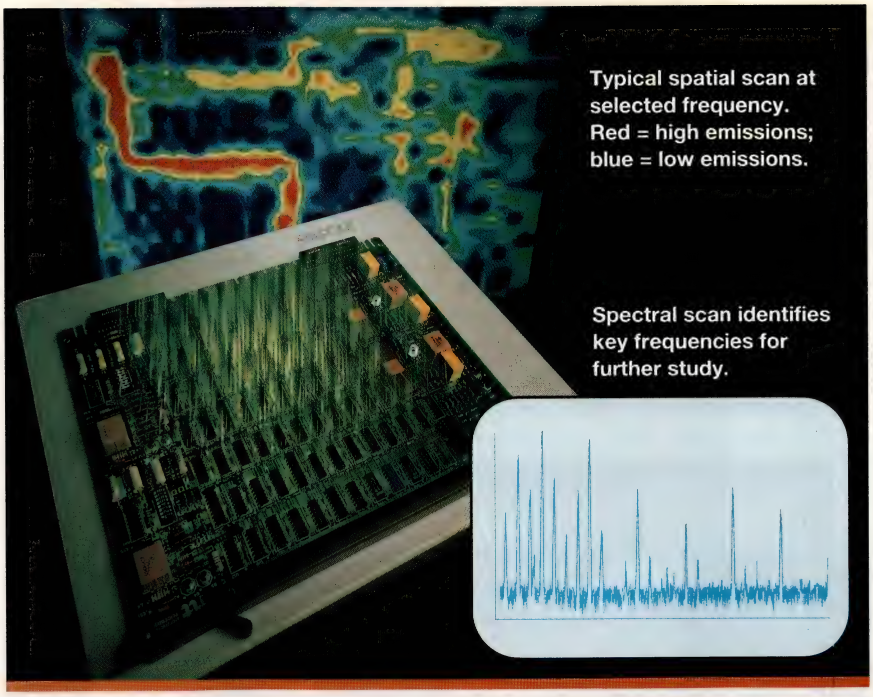
Atlantic Marketing, 12 Galloway Ave., Suite 1B, Hunt Valley, MD 21030; (410) 683-0068. **CIRCLE 685**

X TERMINALS FILL OUT LOW END

The Entry Color X terminal line includes a 14-in. model that costs $1795, a 15-in. unit that sells for $1995, and a 17-in. system that's priced at $2595. All three offer a resolution of 1024 by 768 pixels and a performance measure of 52,000 Xstones.

The ECX family comes with a PCMCIA slot that can accept any compatible card, such as a modem or networking card. A high-speed Centronics-compatible parallel port lets users connect printers or scanners without tying up the terminal's auxiliary serial port. Most standard communication protocols are supported. The systems include 4 Mbytes of DRAM, expandable to 36 Mbytes. RN

Network Computing Devices Inc., 350 North Bernardo Ave., Mountain View, CA 94043; (415) 694-0650. **CIRCLE 686**


Typical spatial scan at selected frequency. Red = high emissions; blue = low emissions.
Spectral scan identifies key frequencies for further study.

Catch emissions problems at board level, where compliance fixes are least costly.

Now you can quickly get a color image of the electromagnetic performance of your printed-circuit board or subassembly *before* final compliance testing. Spatial and spectral displays generated by the EMSCAN PCB emissions scanner show you which frequencies and which areas of the board under test are guilty. These scans are stored for later comparison after design alterations, to check whether offending emissions are now down to acceptable levels.

Just plug your receiver or spectrum analyzer, and your computer with IEEE-488 interface, into the EMSCAN scanner, and a matrix of 1280 H-field probes maps the area of your test board (up to 9" x 12") for high, medium, and low-emissions spots within the 10-to-750-MHz frequency range. Or you can see a spectral display showing the overall condition of the board across the spectrum. You may then choose a frequency of particular interest for intensive spatial examination.

After the development stage, you can use EMSCAN as a quality-control tool, checking completed boards against a "good" scan before they go into assembly. This is the point where production compliance becomes virtually assured.

The software operates under "Windows" to make early diagnosis easy, even for those who are new to compliance testing. It can run on several PCs and workstations, and is readily ported to other environments for analysis.

You should learn all about this qualitative and quantitative measure of emissions for use during product development—where design corrections are least costly. To start, call toll-free (1-800-933-8181) to speak with an applications engineer and arrange to see a demonstration in your office or plant.

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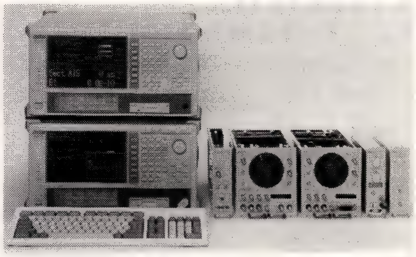
READER SERVICE 82

HANDHELD SCOPE-DMM FEATURES AUTORANGING

The TekMeter is a combination autoranging true-RMS digital multimeter (DMM) and autoranging 5-MHz oscilloscope in a ruggedized 2.2-lb. package. Three versions of the TekMeter are available: the THM 550 (single-channel), THM 560 (dual-channel), and THM 565 (a backlit, dual-channel unit with advanced functions). The DMM features dc and true RMS ranges from 400 mV to 600 V ac and 850 V dc, and ohms ranges from 400 Ω to 40 MΩ. It also does diode and audible continuity tests. Automatic functions include power calculation, transformer harmonic derating factor, variable-speed ac motor control triggering, and line aberration detection. The THM 565 can store 10 waveforms or instrument setups. It also has a real-time clock for time stamping of hard-copy printouts. The THM 550 costs $859, the THM 560 $999, and the THM 565 $1259. All are available immediately. JN

Tektronix Inc., P. O. Box 1520, Pittsfield, MA 01202; (800) 426-2200. **CIRCLE 687**

SDH/SONET ANALYZERS OFFER FLEXIBILE TESTING



The ME3520A/ME3620A SDH/Sonet analyzers allow users to add errors or jitter to the live traffic signal or to overwrite a channel of the live signal with the measurement signal. The analyzers access the network node interface of synchronous multiplexer/demultiplexer systems at 52 Mbits/s, 156 Mbits/s, 622 Mbits/s, and 2488 Mbits/s. They can concatenate signals for large-capacity B-ISDN and ATM telecommunications at STS-3c, STS-12c, and STS-48C. The transmitter and receiver come in separate cabinets, so they can be operated independently. Optical interfaces at wavelengths of 1.31 μm and 1.31/1.55 μm are available as plug-in units. The ME3520A costs $64,875, and the ME3620A costs $77,855. JN

Anritsu Wiltron Sales Co., 685 Jarvis Dr., Morgan Hill, CA 95037-2809; (408) 776-8300. **CIRCLE 688**

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Introducing workstation-level design, simulation and analysis tools for your PC. Intuitive, powerful and dynamic, SystemView thinks like you do. And there's no code to learn! It provides application development tools for DSPs, signal processing, communication and control system applications, plus mathematical system modeling. For more information or to place an order, call ELANIX now.

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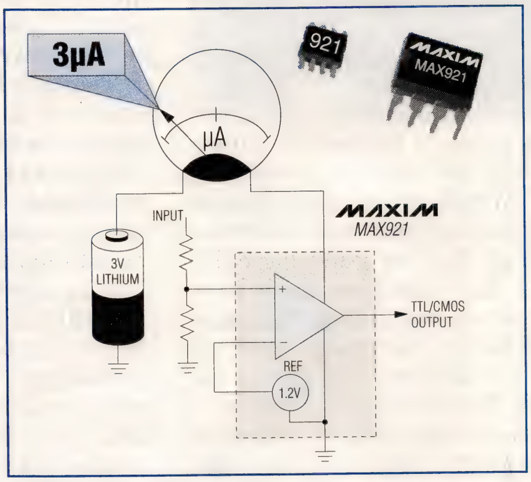
READER SERVICE 130

LOWEST POWER COMPARATORS WITH 1% REFERENCE OPERATE DOWN TO 2.5V

3µA Comparator + Voltage Reference + Adjustable Hysteresis in 8-pin SO

- **3µA Max Supply Current**
- **On-Board 1.2V ±1% Reference**
- **Single Supply: 2.5V to 11V**
  - **Input Range Includes GND**
  - **Dual Supply: ±1.25V to ±5.5V**
- **Adjustable Hysteresis**
  - **No Effect on High-Z Inputs**
  - **Independent of Supply Voltage**
- **TTL/CMOS Compatible Outputs**
  - **No Pull-ups Required**
- **Output Sources 40mA**
  - **12Ω High Side Load Switch**



Operating current for the MAX921 comparator is equivalent to battery leakage current.

Ideal for battery-powered applications, the MAX921 draws less than 3µA from a single lithium cell, with only 12µs prop. delay. The IC includes a 1.2V ±1% reference, and its TTL/CMOS-compatible output requires no pull-up resistor. One pin lets you add hysteresis without affecting the high-impedance inputs. Dual and quad versions are also available.

Choose the Lowest Power Comparators for Battery-Powered Systems

Device		Total Supply Current (µA Max, 25°C)	1.2V Reference Over Temp (% Max)	Adjustable Hysteresis	Package	Price†
MAX921	Single + Reference	3	±1	✓	8-DIP/SO	$1.50
MAX922	Dual	3	N/A		8-DIP/SO	$1.50
MAX923	Dual + Reference	4	±1	✓	8-DIP/SO	$1.95
MAX924	Quad + Reference	7	±1		16-DIP/SO	$2.25

OP AMPS VIDEO & COMPARATORS ANALOG DESIGN GUIDE
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1.2µA Single/Dual/Quad Op Amps Swing Rail-to-Rail!
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Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086, (408) 737-7600, FAX(408) 737-7194.

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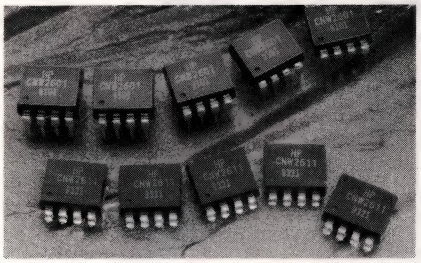
OPTOCOUPLERS MEET VDE 0884 STANDARDS



Three high-speed, VDE-0884-approved, logic-gate optocouplers are targeted for system engineers designing products for the international market. The CNW137, CNW2601, and CNW2611 optocouplers expand HP's family of 10.16-mm- (0.400-in.) wide, 8-pin DIP (or gull-wing SMT) devices. They combine an AlGaAs LED and an integrated, high-gain photodetector. An enable input allows the detector output to be strobed. The detector IC's output is an open-collector Schottky clamped transistor. Pricing in lots of up to 999 ranges from $1.84 for the CNW137 to $3.71 for the CNW2611. Delivery is from stock. DM

Hewlett-Packard Co., Components Div., 370 W. Trimble Rd., San Jose, CA 95131; (800) 537-7715, ext. 7878. **CIRCLE 689**

MICROWAVE AMPLIFIER COVERS 2 TO 8 GHZ

The wide 2-to-8-GHz frequency range is covered by the ZRON-8G medium-power microwave amplifier. The amp features typical power output of 22.5dBm (20 dBm minimum), a maximum VSWR of 2:1, and linear gain of at least 20 dB over the whole band. The hermetically sealed unit is unconditionally stable and withstands transients caused by shorting and/or unshorting a 15-V terminal to the case with full dc applied (1 A external current limiting). Applications include wideband test instrumentation, S- and C-band radars, spread-spectrum and optical communications, and satellite uplinks and line-of-sight transmitting and receiving. Pricing is $495 in single quantities. DM

Mini-Circuits, P.O. Box 350166, Brooklyn, NY 11235-0003; (718) 934-4500. **CIRCLE 690**

12-LED ARRAY OFFERS SLEEK LOOK

Applications in modems and fluid-level and telecom-status indicators are possible for the 550-0012-801 rectangular array of 12 LEDs. The device's sleek low profile assures consistent lead alignment and lower insertion costs. The unit operates from –55 to 100°C and offers a 110° viewing angle with a typical luminous intensity of 3.5 mcd. The LEDs are packaged in a UL 94V0-rated black housing for maximum contrast ratio. Offered in standard 20-mA red, the array can also be ordered in custom color combinations. Pricing starts at $2.25 for lots of 1000. DM

Dialight Corp., Dept. ARAY, 1913 Atlantic Ave., Manasquan, NJ 08736; (908) 223-9400. **CIRCLE 691**

You Need Tree City USA

City trees add the soft touch of nature to our busy lives. They cool our cities, fight pollution, conserve energy, give wildlife a home, and make our neighborhoods more liveable.

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You can make a difference — by planting and caring for trees in your yard and in your neighborhood, and by encouraging your city government's community forestry program.

Support Tree City USA where you live. For your free booklet, write: Tree City USA, The National Arbor Day Foundation, Nebraska City, NE 68410.

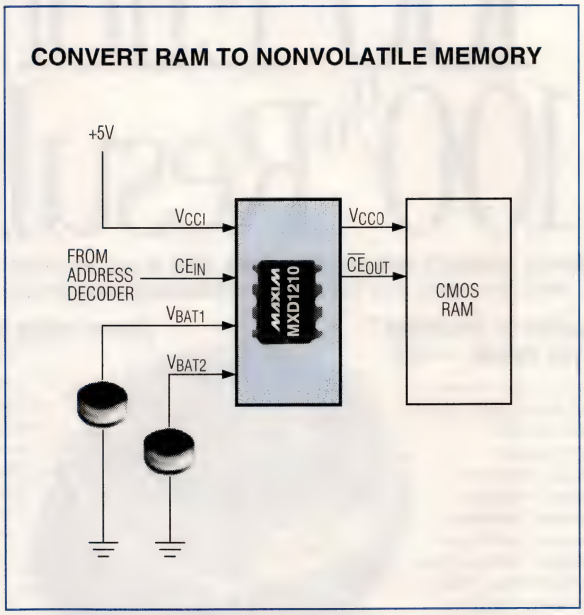
The National Arbor Day Foundation

RAM PROTECTION IC CONSUMES ONLY 230µA

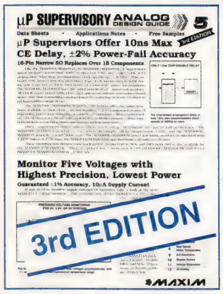
Write Protection & Battery Backup in an 8-pin SOIC

The MXD1210 converts CMOS RAM into nonvolatile memory by connecting the higher of two backup batteries to the RAM V_{CC} during power failures. By gating the RAM's enable signal $\overline{CE}$, the MXD1210 prevents spurious write operations during power failures.

- **Low I_{SUPPLY} –**
  230µA in Operating mode
  2nA in Backup mode
- **Backup Switchover With Redundant Battery Option**
- **20ns max Chip Enable Prop Delay**
- **5% or 10% power fail trip thresholds**
- **Smallest package – 8-pin SOIC**
- **Second-source to DS1210 available in 8-pin DIP or 10-pin SOIC**



Like the DS1210, the MXD1210 provides backup-switchover and chip-enable gating. But power consumption is 10X lower, and the 8-pin SOIC package is only 1/4 the size of the DS1210 16-pin SOIC.



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16-Pin Narrow SO Replaces Over 15 Components

Monitor Five Voltages with Highest Precision, Lowest Power

Guaranteed ±1% Accuracy, 10µA Supply Current

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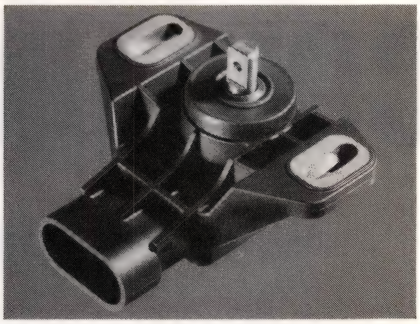
READER SERVICE 136

CONTACTLESS SENSOR MEASURES POSITION

A fully encapsulated, non-wearing, and adjustment-free solution to angular position measurement is offered by the KMA10/70 contactless sensor. The device is applicable to many automotive and industrial tasks such as active-suspension units, accelerator-pedal position sensing, and servo-controlled actuators. Based around Philips's KMZ11B1 magneto-resistive sensor element, the sensor has an integral input shaft, sealed bearing, and magnet assembly, which allow the magnet's magnetic field to be rotated over the sensor element. The resultant changes in the sensor element's resistance are detected by a thick-film hybrid signal-conditioning circuit, which produces a temperature-compensated 4-to-20-mA output signal that corresponds to the angular displacement of the input shaft. The three-terminal device operates over a voltage range of 8.1 to 11 V. Call for pricing and delivery. DM

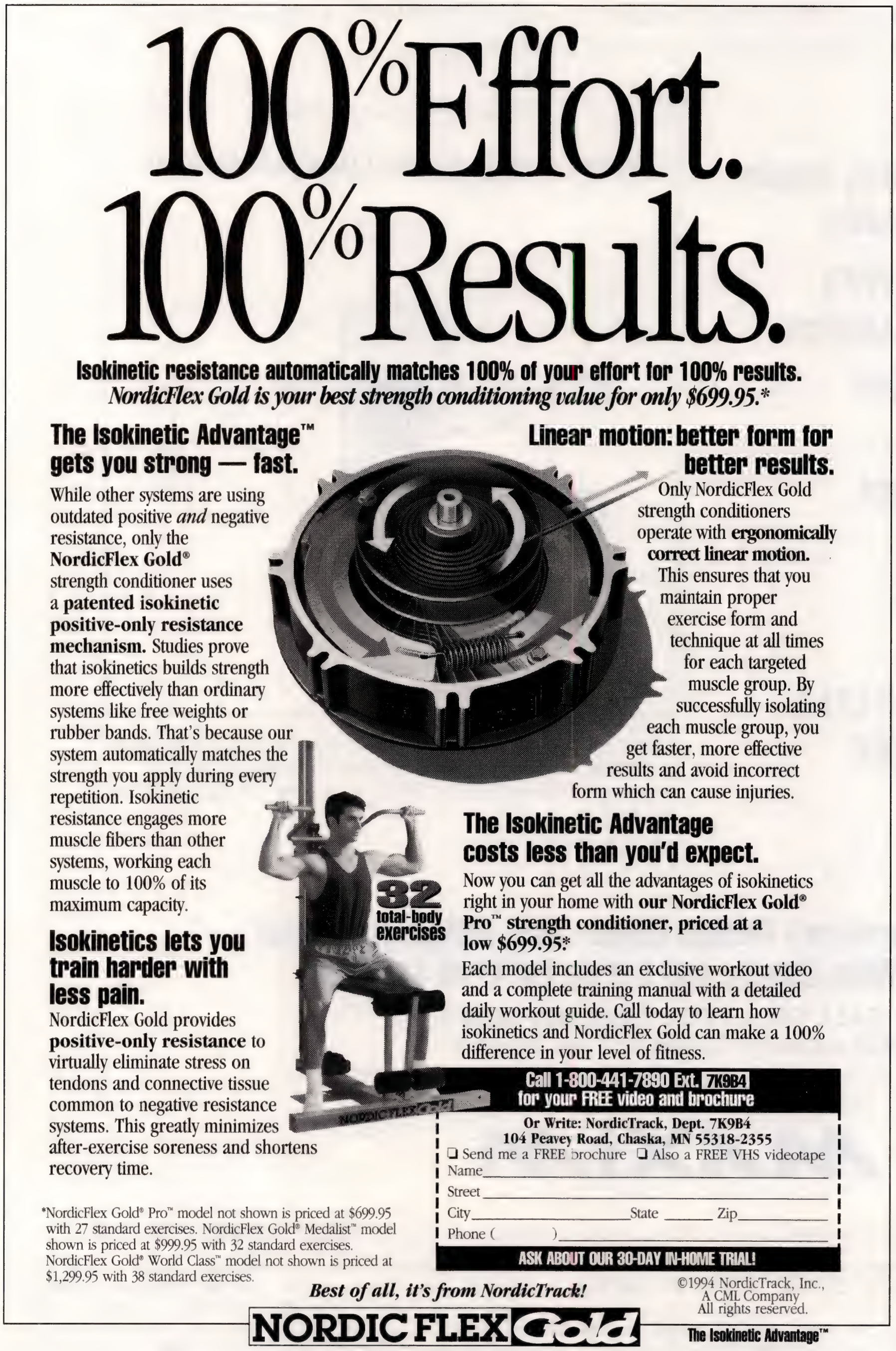


Philips Semiconductors, Discrete Product Div., P.O. Box 10330, Riviera Beach, FL 33404; (800) 447-3762. **CIRCLE 692**

SUBMINI VOLTMETER BOASTS DUAL RANGES

A line of 4-1/2-digit subminiature digital voltmeters comes encapsulated in standard plastic DIP packages measuring 0.9 by 2.1 by 0.43 in. The DMS-40LCD Series of voltmeters offers dual-input-range capability, allowing signal-input coverage from ±200 mV to ±200 V in pairings of ±200 mV/±2 V, ±2 V/±20 V, or ±20 V/±200 V. The large 0.4-in., easy-to-read LCD display combined with the devices' compact size makes them suitable for use in automatic test equipment, portable instruments, and more. Backlit and non-backlit models are offered. The meters operate efficiently from a single +5-V or +9-V source. Pricing starts at $79. Delivery is from stock. DM

Datel Inc., 11 Cabot Blvd., Mansfield, MA 02048; Tony Keirouz, (508) 339-3000, ext. 291. **CIRCLE 693**



100% Effort.
100% Results.

Isokinetic resistance automatically matches 100% of your effort for 100% results.
*NordicFlex Gold is your best strength conditioning value for only $699.95.**

The Isokinetic Advantage™ gets you strong — fast.

While other systems are using outdated positive *and* negative resistance, only the **NordicFlex Gold®** strength conditioner uses a **patented isokinetic positive-only resistance mechanism.** Studies prove that isokinetics builds strength more effectively than ordinary systems like free weights or rubber bands. That's because our system automatically matches the strength you apply during every repetition. Isokinetic resistance engages more muscle fibers than other systems, working each muscle to 100% of its maximum capacity.

Linear motion: better form for better results.

Only NordicFlex Gold strength conditioners operate with **ergonomically correct linear motion.** This ensures that you maintain proper exercise form and technique at all times for each targeted muscle group. By successfully isolating each muscle group, you get faster, more effective results and avoid incorrect form which can cause injuries.

Isokinetics lets you train harder with less pain.

NordicFlex Gold provides **positive-only resistance** to virtually eliminate stress on tendons and connective tissue common to negative resistance systems. This greatly minimizes after-exercise soreness and shortens recovery time.

32 total-body exercises

The Isokinetic Advantage costs less than you'd expect.

Now you can get all the advantages of isokinetics right in your home with **our NordicFlex Gold® Pro™ strength conditioner, priced at a low $699.95.***

Each model includes an exclusive workout video and a complete training manual with a detailed daily workout guide. Call today to learn how isokinetics and NordicFlex Gold can make a 100% difference in your level of fitness.

Call 1-800-441-7890 Ext. 7K9B4 for your FREE video and brochure

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ASK ABOUT OUR 30-DAY IN-HOME TRIAL!

*NordicFlex Gold® Pro™ model not shown is priced at $699.95 with 27 standard exercises. NordicFlex Gold® Medalist™ model shown is priced at $999.95 with 32 standard exercises. NordicFlex Gold® World Class™ model not shown is priced at $1,299.95 with 38 standard exercises.

Best of all, it's from NordicTrack!

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NORDIC FLEX Gold
The Isokinetic Advantage™

READER SERVICE 1

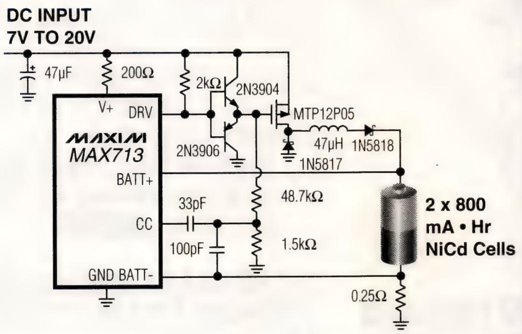
FAST-CHARGE NiCd & NiMH BATTERIES IN UNDER 1 HOUR

Safe and Reliable Solution Needs Only Low-Cost Components

The MAX712 and MAX713 are complete battery charging systems in a single IC. Each contains an A/D converter, analog power control ciruitry, and all the intelligence necessary to safely and reliably fast-charge and trickle-charge Nickel-Cadmium or Nickel-Metal-Hydride batteries. Automatic switch-over from fast-charge to trickle-charge protects batteries. So do user-set charge rates, temperature detection points, and time-out periods.

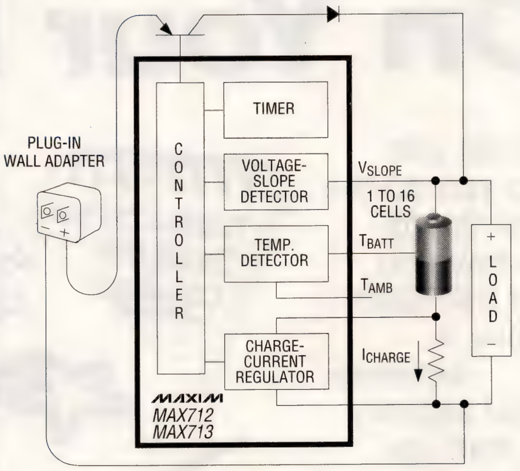
- **Charge 1 to 16 Cells in Series**
- **Needs Only Low-Cost Components**
- **Voltage-Slope, Temperature, and Time-Out Detection**
- **Fast-Charge at 4C to C/3 Rates (15 minutes to 3 hours)**
- **Trickle-Charge at C/16 Rate (16 hours)**
- **16-Pin Narrow SOICs and DIPs**
- **Complete Evaluation Kit***
- **Only $3.10****

4A SWITCH-MODE APPLICATION USES FEWEST COMPONENTS



LINEAR CURRENT-REGULATION APPLICATION

FAST-CHARGER NEEDS ONLY A PNP, DIODE, AND LOW-COST PASSIVES



The MAX712 and MAX713 determine fast-charge termination using a sophisticated combination of voltage-slope, temperature, and time-out detection. The MAX712 uses zero-slope detection; The MAX713 uses negative-slope detection.

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READER SERVICE 137

SOUND BOARD EMPLOYS WAVE-TABLE SYNTHESIS

Wave-table synthesis is the technology behind the SoundMan Wave, a 16-bit stereo sound board. Wave-table synthesis is done using true instrument recordings rather than computer-generated sounds, resulting in more realistic sounds. In addition, a proprietary MIDI interpreter lets users hear wave-table quality in many popular games. The SoundMan Wave offers 44-kHz sampling, 44 wave-table and FM voices, a SCSI CD-ROM interface, and a five-channel stereo mixer. Windows 3.1 and DOS are both supported. A host of software applications are bundled with the board as well. It is priced at $349. RN

Logitech Inc., 6505 Kaiser Dr., Fremont, CA 94555; (510) 795-8500. **CIRCLE 694**

INDUSTRIAL CONTROLLER IS BASED ON STD 32

A compact STD 32 platform packs a 486 microprocessor, 32-bit local-bus video, an 80-Mbyte hard-disk drive, and a power supply in a space that's under 3-in. wide. Suited for embedded applications, the microCat industrial computer can handle 486 CPUs from 25 to 66 MHz. The processor board also holds up to 8 Mbytes of DRAM, 2 Mbytes of flash memory, and several I/O options. A dual PCMCIA 2.0 interface is available for applications that require rugged removable media. Systems that don't require the high speed offered by the local-bus video can eliminate that feature to reduce the system cost. Power is supplied through a plug-in dc-to-dc power-supply single-slot board, which accepts most standard voltage levels. A basic unit, with a 25-MHz 486SX, 4 Mbytes of DRAM, DOS 5.0 stored in flash, a Super VGA controller, an 80-Mbyte drive, and a power-supply board, starts at $3290. Large-quantity discounts are available. RN

Ziatech Corp., 3433 Roberto Ct., San Luis Obispo, CA 93401; (805) 541-0488. **CIRCLE 695**

PARALLEL-PROCESSING BOARD HOLDS 16 DSPS

Up to 16 DSP processors fit on the CNAPS/VME-16 VME board. Designed for parallel-processing applications, the 6U board delivers 1.3 BOPS at 20 MHz. The board employs a single-instruction, multiple-data (SIMD) architecture that acts as a coprocessor to perform high-speed parallel operations. Each processor contains a multiplier, adder/accumulator, a shifter-logic unit, and on-chip RAM. In quantities of 100, the CNAPS/VME-16 sells for $3900. A 32-processor version is priced at $5850. Both models are available now. RN

Adaptive Solutions Inc., 1400 N.W. Compton Dr., Suite 340, Beaverton, OR 97006; (503) 690-1236. **CIRCLE 696**

Put Our List On Your List

THINGS TO DO: Send for Catalog!

Consumer Information Catalog

Our list can help you do the other things you have on your list. Such as buy a car. . . estimate social security . . . start the diet. . . check out investments. . .

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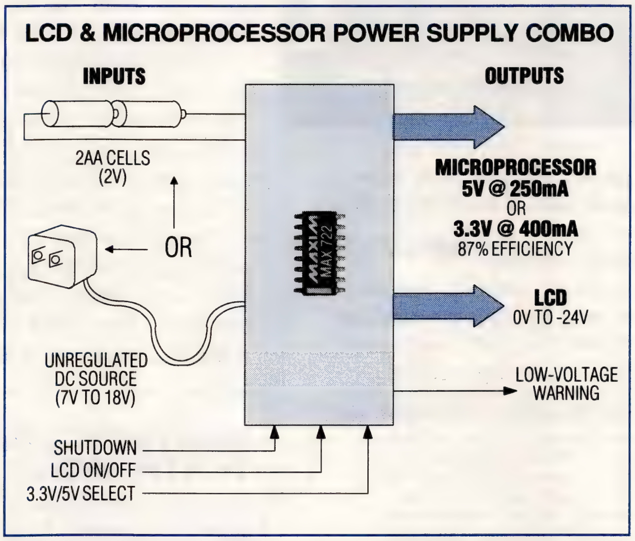
SINGLE CHIP LCD & PROCESSOR SUPPLY HAS 87% EFFICIENCY

Regulated 3V or 5V and 0V to -24V From a 2V Battery

The MAX722/MAX723 dual-output switching regulators provide an unbeatable combination of high efficiency, low supply current, and small size. They fit perfectly in your palmtop computer and other battery-powered equipment designs. Integrated features include low-voltage warning and automatic switching between battery-power and wall adapter power.

- **Main Output**
  - **3.3V or 5V – MAX722**
  - **3V or 5V – MAX723**
- **LCD Output: 0V to -24V**
- **87% Efficiency**
- **60µA Quiescent Current**
- **20µA Shutdown Mode**
- **Logic-Controlled Outputs**
- **Small 16-Pin SOIC**
- **$5.45***


LCD & MICROPROCESSOR POWER SUPPLY COMBO
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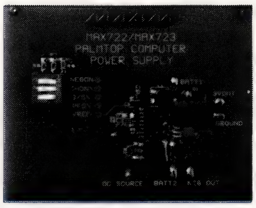
OUTPUTS
2AA CELLS (2V)
OR
MAXIM MAX722
MICROPROCESSOR 5V @ 250mA OR 3.3V @ 400mA 87% EFFICIENCY
LCD 0V TO -24V
UNREGULATED DC SOURCE (7V TO 18V)
LOW-VOLTAGE WARNING
SHUTDOWN
LCD ON/OFF
3.3V/5V SELECT



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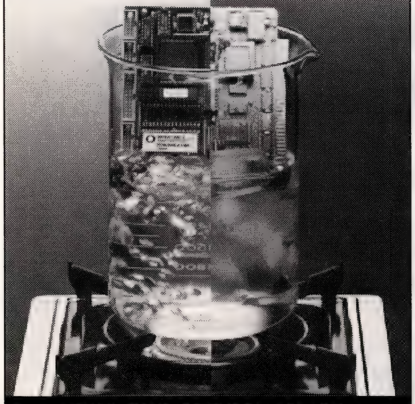

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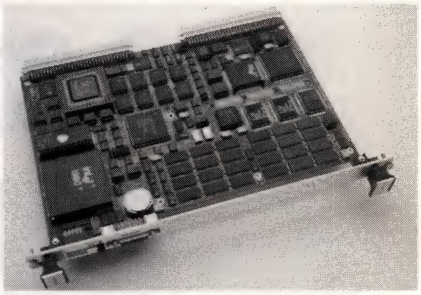
VME64 BOARD TARGETS GRAPHICS APPLICATIONS

Based on a 32-bit i960CF RISC microprocessor, the HK80/V960D has the power to handle graphics-oriented applications, such as image processing and simulation. The 30-MHz board fits a VME form factor and features a 54-Mbyte/s VME64 system bus interface. In addition, it comes with 16 Mbytes of DRAM, 4 Mbytes of flash memory, four serial ports, a socket that can hold up to 512 kbytes of ROM, and on-board Ethernet.

Customization is handled through a 32-bit, 200-Mbyte/s mezzanine-board interface. The interface is handled as an open specification. As a result, designers can build their own I/O, memory, or processor modules.

Complimenting the V960D's internal high-speed data-movement capability is a DMA-intensive I/O architecture. The 64-bit mater/slave VME64 interface is based on a Cypress VIC64 VME interface IC. To further boost VME throughput, FIFO buffers decouple the mezzanine and VMEbus interfaces, letting both run at their maximum speed.



Software support for the board includes VxWorks and a series of utilities for debugging and diagnosis. With 8 Mbytes of DRAM, the HK80/V960D sells for $4495.

***Heurikon Corp.**, 8310 Excelsior Dr., Madison, WI 53717; (800) 356-9602 or (608) 831-0900.*

CIRCLE 697

■ *RICHARD NASS*

CONVERT VGA OUPUT TO NTSC SIGNAL

In many instances, a computer display is too small to be viewed by an entire audience. Using TapeIT! Portable, a VGA-to-VCR/TV converter box, large-size television monitors or projection systems can be connected to the display. The images are then shown simultaneously on both the PC display and the external device. The converter box does this by converting the PC's VGA output to an NTSC signal. A proprietary algorithm results in a flicker-free video image. Another use for the TapeIT! Portable is to connect a VCR directly to a PC, eliminating the need for a camera. The converter sells for $539 and is available now. RN

New Media Graphics Corp., 780 Boston Rd., Billerica, MA 01821; (508) 663-0666. **CIRCLE 698**

FRAME GRABBER HANDLES 5 TO 160 MHZ

The HI*DEF III is a high-speed frame grabber that's been ported to the VMEbus from the PC. The 160-MHz board is fully programmable and can capture images from either analog or digital video sources. The high bandwidth makes the board suitable for medical, military, and industrial applications. Up to 8 Mbytes of video RAM fits on the board. Using multiple passes and inputs, true-color (24-bit) images can be captured, either interlaced or non-interlaced. The board's analog architecture helps reduce jitter, drift, noise, and crosstalk while increasing stability. The HI*DEF III sells for $5990. A digital-only board costs $3995. OEM discounts are available. RN

Imagraph Corp., 11 Elizabeth Dr., Chelmsford, MA 01824; (508) 256-4624. **CIRCLE 699**

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SIMULATION, SYNTHESIS JOIN LOW-COST TOOLSET

Viewlogic has added VHDL simulation and synthesis to its low-cost PRO Series of design tools for the PC. The PROvhdl and PROsynthesis modules complete the company's top-down environment for FPGA and complex PLD design. The VHDL simulator is IEEE 1076 compliant, and extends the capabilities of Viewlogic's existing digital simulator to handle register-transfer-level and behavioral descriptions. PROsynthesis takes in a VHDL description and produces a gate-level representation targeted at a specific FPGA or complex PLD family. Architecture-specific algorithms ensure an integrated flow from initial design description through vendor-specific place and route. The PRO Series tools run on a PC under Windows. PROvhdl and PROsynthesis cost $1995 and $4995, respectively. Users can purchase the tools as standalone modules, or integrated with the other PRO Series tools. LM

Viewlogic Systems Inc., 293 Boston Post Rd. West, Marlboro, MA 01752-4615; (508) 480-0881.

CIRCLE 700

USE ESDA TOOL TO DRAW VERILOG DESCRIPTIONS

Engineers can use the DesignVision software to graphically create Verilog synthesis and simulation models. Verilog users "draw" behavioral models by graphically describing the events and corresponding reactions of a model. DesignVision represents models as a collection of threads. Each thread depicts a series of events and actions. As each event occurs during simulation, the corresponding action is performed. All threads are active (in other words, simulate) at the same time. This style of modeling makes it easy to see and understand separate operations that occur simultaneously. Users can generate two types of Verilog code: a behavioral style for simulation, and two styles of RTL descriptions for synthesis. DesignVision for Verilog is shipping now for $15,000. It runs on Unix workstations. LM

Vista Technologies Inc., 1100 Woodfield Rd., Schaumburg, IL 60173; (708) 706-9300. **CIRCLE 701**

SPICE LIBRARY UPDATE INCLUDES PIN DIODES

The latest update to Intusoft's Spice model library for RF devices includes several new types of models, such as PIN diodes, MMICs, GaAs MESFETs, and an ideal coupler. The new library, with over 200 additions, is three times as big as the previous version. The models can be used with any Berkeley-Spice-compatible simulator on any computer platform. Unlike some RF Spice models, the Intusoft models don't use unrealistic parameters to force-fit the device behavior. Instead, a custom subcircuit approach is used that accounts for all package parasitics, and matches the published s-parameter magnitude and phase data. As a result, any Spice program can simulate linear and nonlinear RF circuits using frequency-, dc-, and time-domain analyses. Several test circuits are included with the library. RF Device Library Version 3.0 is available on floppy disk in DOS and Macintosh formats. The library costs $150. LM

Intusoft, P.O. Box 710, San Pedro, CA 90733-0710; (310) 833-0710. **CIRCLE 702**

MODEL LIBRARY HELPS BUILD WIRELESS DESIGNS

A library of more than 65 functional blocks for designing communications systems is now available to support the DSP Framework design environment from Comdisco Systems. DSP Framework has a block-diagram-based graphical user interface that lets users create, simulate, and implement a DSP design through a set of push buttons and pull-down menus. The communications library contains such elements as modulators, demodulators, adaptive equalizers, and wireless channels that are suited for digital cellular phones, pagers, mobile communications, satellite-based systems, and other wireless applications. Two digital-cellular demonstration systems can be used as tutorials or starting points for new designs. DSP Framework runs on Unix workstations. The communications library costs $5000 for the first node. LM

Comdisco Systems Inc., 919 E. Hillsdale Blvd., Foster City, CA 94404; (415) 574-5800. **CIRCLE 703**

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POWER-FACTOR ICs CHECK LINE DISTORTION

When installed in power supplies, two power-factor-correction ICs, the LT1248 and LT1249, eliminate line-current distortion in ac-power lines and help supply manufacturers bring their products in line with IEC 555-2 specifications. Both use fixed high-frequency pulse-width-modulation current averaging and require no slope compensation. This approach enables the ICs to achieve lower line-current distortion and to use lower-cost switches and magnetics than ICs or systems that rely on either peak-current detection or zero-current switching. The LT1248 is for operation at frequencies up to 300 kHz, while the LT1249 has an internally fixed switching frequency of 100 kHz. However, the LT1249 uses only eight pins and is in a smaller package. Typical startup supply current is 250 μA with quiescent current of just 9 mA. Pricing for the LT1248 is $3.53 in a 16-pin plastic DIP and $3.76 in a 16-lead SOIC. The LT1249 costs $3.19 in an 8-pin DIP and $3.44 in an 8-lead SOIC. All prices are for lots of 1000. Samples are available now. DM

Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035-7487; (800) 4-LINEAR. CIRCLE 704

DC-DC CONVERTERS CAN BE WASHED DOWN

A hard-potting method is used to protect the XT and NT Series of dc-dc converters from moisture damage during water-washing processes used to clean printed-circuit boards. Each converter is hard-epoxy potted to the header, which is sealed with a double adhesive. The XT Series puts out 50 to 60 W in a 3-by-2.58-by-0.83-in. case. It comprises 5-, 12-, and 15-V single-output types. The NT Series packs 10 W into a 1-by-2-by-0.4-in. case and 20 W into a 2-by-2-by-0.45-in. case. NT converters come with single or dual outputs. Nominal input voltages for both series are 12, 24, or 48 V. All models in the series carry a five-year warranty. Call for pricing and delivery information. DM

Calex Mfg. Co. Inc., 2401 Stanwell Dr., Concord, CA 94520; Stu Williams, (800) 542-3355. CIRCLE 705

200-W CONVERTERS SPORT 300-V INPUT

A 300-V-input version of the BASIX family of high-density dc-dc converters is available. Using the company's resonant transition zero-voltage-switching topology and integrated magnetics in a 4.6-by-2.4-by-0.5-in. package, the converters provide a usable power density of 36 W/in.^{2} with efficiencies of up to 87%. In addition, the unit's 700-kHz fixed frequency and proprietary topology cut internal noise to within VDE0871 Class A specs with no external filtering. Peak-to-peak output ripple is below 1%. Units are available in 48-V narrow (40 to 60 V) and wide (36 to 75 V) input ranges with standard output voltages of 3.3, 5, 12, 15, 24, and 48 V dc. A 300-V wide-input (200 to 400 V) version is sampling now. OEM pricing starts at $160. DM

Computer Products, Power Conversion America, 7 Elkins St., South Boston, MA 02127; (617) 268-1170. CIRCLE 706

DENSE CONVERTERS COVER UP TO 20 W

The OHD2800S Series of dc-dc converters is a line of single-ended, forward-converter units rated up to 20 W of output power over the full military temperature range with outputs of +5, +12, and +15 V. The fixed-frequency units use a resonant transformer-reset circuit which allows for a maximum duty cycle of 67% without increasing the voltage stress on the primary MOSFET or output rectifiers. Tight line and load regulation are achieved through a wide-bandwidth magnetic-feedback circuit. Other features include constant-frequency pulse-width-modulation design, 81% efficiency at full load, and a wide input range of 16 to 40 V dc. Two synchronization options are offered. Pricing is $325 in lots of 100. Delivery is from stock to eight weeks. DM

Omnirel Corp., 205 Crawford St., Leominster, MA 01453; (508) 534-5776. CIRCLE 707

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Model	LO/RF IF (MHZ)	CONV. LOSS	ISOLATION LO-IF
TDM-1103L	10-1000 DC-1000	TYP. 7dB	> 22dB
TDM-1213L	1-1200 DC-1000	TYP. 7.5dB	> 20dB
TDM-1203L	10-1200 DC-1000	TYP. 8dB	> 22dB
TDM-1803L	150-1800 DC-1000	TYP. 8dB	> 21dB
TDM-2003L	150-2000 DC-1000	TYP. 8dB	> 19dB

• Freq. Doublers

Model	Ft (MHZ) RANGE	Input Power	out F2	out F1	out F3
TFD-13	1-500	0 ~ + 10dBm	< 14dB (0dBm)	>22dB	>35dB

• Power Splitters

Model TSP-	Ft (MHZ) RANGE	INSERT LOSS	AMPL. UNBAL.	ISOLA TION	VSWR
0713	2-700	< 1.5dB	< 0.5	>19.0	1.5:1

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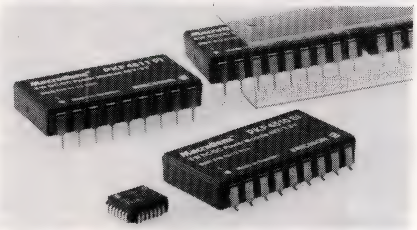
A series of 15-W isolated dc-dc converters is claimed to have the smallest footprint commercially available. The PT31 converters owe their small size to a switching frequency of more than 650 kHz and the use of planar magnetics and surface-mount construction. The devices boast a power density of 15 W/in.^{3} and measure 1.45 by 1.64 by 0.38 in. Their efficiency is rated at 80%. Two units are initially available: the PT3101A is a 48-to-5-V unit, and the PT3102A is a 48-to-12-V converter. Both operate over an input range of 36 to 72 V dc, and neither requires a heat sink to deliver its rated power. Line regulation is ±0.2% and load regulation is ±0.4%. Pricing in lots of 100 is $55. Delivery is in 60 to 90 days. DM

Power Trends Inc., 1101 N. Raddant Rd., Batavia, IL 60510; (708) 406-0900. **CIRCLE 708**

DC-DC MODULES MOUNT WITH AUTOMATIC EASE

A DIP-housed dc-dc module that weighs just 15 grams is suitable for automatic insertion into systems based on free-convection-cooled distributed-power architectures. The MacroDens series of converters gives designers an economical route to the advantages of distributed power in 48/60-V, battery-backed systems. Four initial models comprise the line with output voltages and power levels of 2 V/3 W, 3.3 V/5 W, 5 V/6 W, and 12 V/7 W. The 5-V version is 83% efficient and stands just 8 mm tall. An MTBF specification of over 400 years (3.5 million hours) results from a low component count, hybrid technology, and a high degree of silicon integration. Samples are available from stock. High-volume pricing is below $20. DM



Ericsson Components, P.O. Box 853904, Richardson, TX 75085-3904; Anders Hansson, (214) 907-7906. **CIRCLE 709**

5-W CONVERTERS MEET MIL SPECS

The low-profile, 5-W MSA Series of dc-dc converters is available on Standard Military Drawings (SMDs) and meet all requirements for MIL-H-38534, Class B-qualified hybrids. The military hybrid requirements define component quality, workmanship standards, qualification testing, and screening procedures to ensure high reliability. The converters come in a welded metal case measuring 1 by 1 by 0.27 in. They handle continuous input voltages from 16 to 40 V dc. Output voltages are available at 5, 12 (single or dual), or 15 V dc (single or dual). Pricing is $630 in lots of 100. Delivery is stock to eight weeks. DM

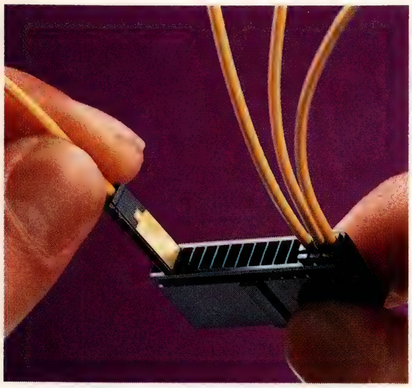
Interpoint Corp., 10301 Willows Rd., P.O. Box 97005, Redmond, WA 98073-9705; (206) 882-3100. **CIRCLE 710**

POWER MODULES REJECT NOISE

An improvement to the low-power Intellimod line of intelligent power modules provides improved noise immunity and allows users to eliminate the use of certain external capacitors. The PMxxCMA060 devices replace the PMxxCHA060 Series and range from 10 to 30 A at 600 V. The new family maintains the same compact package and pinout for easy interchangeability. The improved noise immunity, combined with standard protection features, makes for higher system reliability and lower overall cost. Prototypes are available from stock to six weeks with production lots running eight to 12 weeks. A typical price is $49.53 for 10 pieces of the PM10CMA060 module (600 V at 10 A). DM

Powerex Inc., 200 Hillis St., Youngwood, PA 15697; Joe Cancilla, Sr., (412) 925-4488. **CIRCLE 711**

Controlled Impedance Ground Plane Interconnects (GPI™) are Designed to Exceed 1 GHZ System Speeds



Meritec's new Ground Plane Interconnects are engineered to match impedance and propagation rate while minimizing crosstalk. The assemblies are impedance matched from the board through the assembly and designed to reduce signal-to-signal crosstalk. The assemblies are designed for CMOS, ECL or GaAs logic and can handle system speeds exceeding 1 GHZ with 35 picosecond rise times. A passive latch connects the termination to the housing or to a carrier system. Meritec's precision terminations are highly reliable in critical applications.

Circle 92

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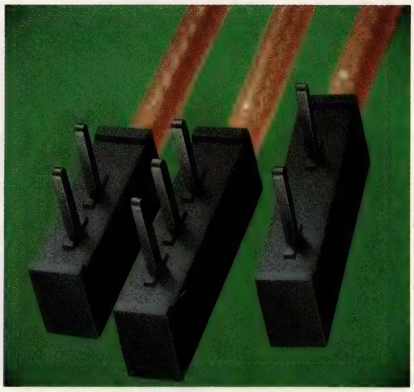
Circle 95

Impedance Matched and Overmolded SCSI Cable Assemblies

Meritec's 68 position SCSI female-to-female cable assemblies are designed for applications requiring high speed, performance and reliability. Standard cable impedances of 85, 90, 95 and 100 ohms are available. The low profile connectors are terminated to FEP cable and overmolded for strain relief to provide for bused grounds to customer designated pins. Terminations are mass soldered for high reliability. In addition to the female-to-female configuration, male-to-male and male-to-female versions are available on standard SCSI .050" x .100" spacing. Circle 93

Low Profile Impedance Matched PCB Solderable Interconnects



Meritec's low profile, impedance matched PCB Solderable Interconnects solder directly to the PCB for a permanent connection. Pin lengths of .110" and .160" are available for different board thicknesses. The connectors feature precision, high strength molded terminations for reliability in critical applications. Available in 1x2 and 1x3 configurations, the connectors are side-to-side stackable and feature heights as low as .150" from the PCB, making them ideal for dense package applications. A variety of different cable styles are available for the assemblies.

Circle 94

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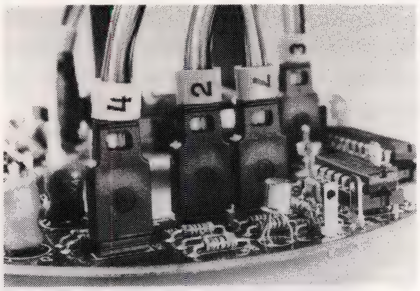
A series of subminiature connectors with 2-mm-pitch spacing for high-density industrial applications is available. The SP Series connectors are single-row, wire-to-board types based on the European 2-mm grid.



The pc-board socket headers are offered in from two to six positions and are polarized for proper mating of the male connector. A keying system is also offered to prevent mismating. Male connectors are supplied premolded to either jacketed cable, ribbon cable, or twisted pair in either straight or right-angle versions. Pricing for a model SPSG66FA six-conductor cable assembly with connector is $3.11 in lots of 1000. Delivery is from stock to six weeks. DM

Richard Hirschmann of America Inc., Industrial Row, P.O. Box 229, Riverdale, NJ 07457; (800) 225-0254, ext. 230. **CIRCLE 712**

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By packaging its ACT 1 family of field-programmable gate arrays (FPGAs) in very thin quad flat packs (VQFPs), Actel offers an answer to designers of PCMCIA cards, notebook computers, or other applications restricted by height or surface requirements. The A1010B and A1020B FPGAs are 1200- and 2000-gate devices, respectively, and are intended to provide optimum capacity for applications in which medium amounts of logic must be integrated. Available in a 1-mm-tall, 80-pin package, the arrays offer a small footprint of 16 by 16 mm and a pin pitch of 0.65 mm. Pricing for the A1010B and A1020B arrays in lots of 5000 is $13.80 and $21, respectively. Small quantities are from stock. DM

Actel Corp., 955 E. Arques Ave., Sunnyvale, CA 94086; (408) 739-1010. **CIRCLE 713**

ELEVATOR SOCKET RAISES DISPLAYS

A 10-pin, elevated-height socket with 0.200-in. row-to-row spacing increases the visibility of LEDs and other display devices within the end-user's chassis. The P/N 10-28440-10 socket lifts displays with 0.200-in. spacing to a height of 0.440 in. above the pc board. Other above-board heights are available with a modest tooling fee. The socket features bifurcated, stamped three-point contacts designed to mate perfectly with flat or flimsy display leads. Pricing is $0.80 in lots of 1000 with delivery in six weeks. DM

Aries Electronics Inc., P.O. Box 130, Frenchtown, NJ 08825; Frank Folmsbee, (908) 996-6841. **CIRCLE 714**

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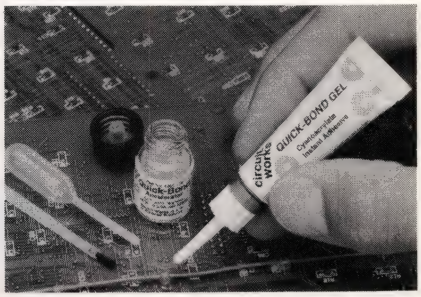

Planned Products, 303 Potrero St., Suite 53, Santa Cruz, CA 95060; (408) 459-8088. **CIRCLE 715**

DATA COMPRESSOR EXPANDS OUTPUT

The Series 5000 LAN/WAN Optimizer, an advanced data-compression device, increases the throughput of a bridge, router, front-end processor, or channel extender two to four times (on average), depending on the type of information being transmitted. It uses an advanced hardware pipeline and multiprocessor architecture to minimize compression/decompression latency and maximize throughput. Increased throughput significantly reduces bandwidth requirements and enables the use of lower links. It also reduces congestion of the WAN.

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***Telco Systems, Inc.**, Magnalink Communications, 63 Nahatan St., Norwood, MA 02062; (617) 255-9400 or -5885.* **CIRCLE 716**

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The Integrated Access Node, a flexible branch internetworking product, consolidates SNA/legacy and LAN traffic by combining multiprotocol routing with Frame Relay and X.25 switching. IAN's release coincides with that of the SNMP-based Element Management System (EMS), which provides integrated management of SNA/legacy and LAN traffic. Ideal for branch office use or in remote sites, the IAN provides the advantages of switching and routing via a connection-oriented networking architecture. The result is seamless support for connectionless LAN protocols, and connection-oriented IBM/legacy protocols over connection-oriented technologies, such as X.25, Frame Relay, and soon, ATM. The standards-based IAN routes all major LASN protocols including TCP/IP, IPX, DECnet IV, OSI, XNS, and Apple Talk, and bridges other protocols utilizing transparent bridging, source routing, and spanning tree. The IAN also provides an integrated solution for Asynchronous and Synchronous protocols, including SNA/SDLC, BiSync, and Burroughs Poll Select.

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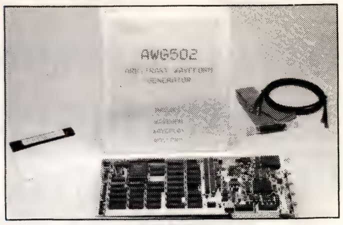

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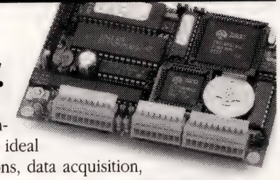

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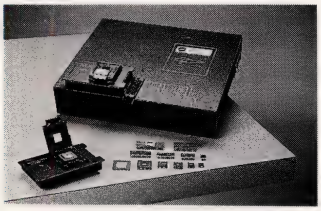

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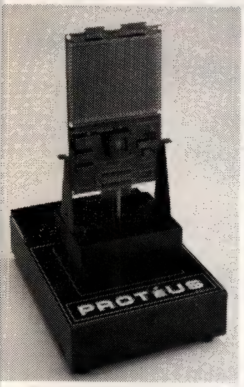

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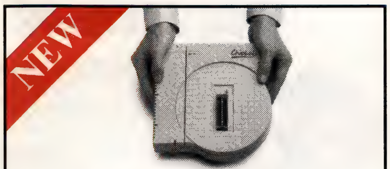

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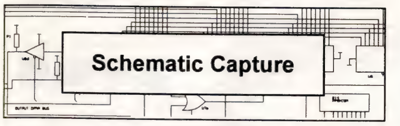

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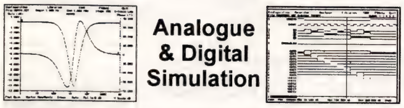

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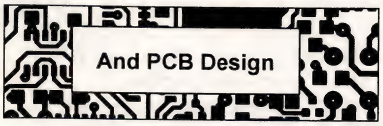

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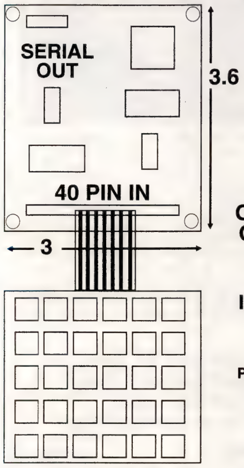

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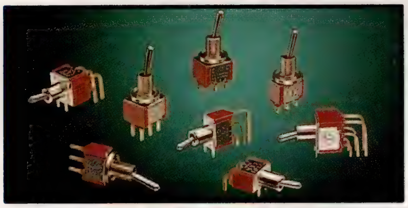

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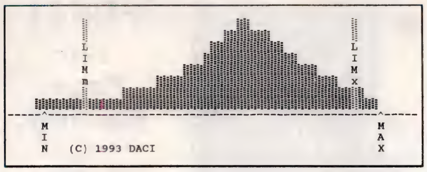

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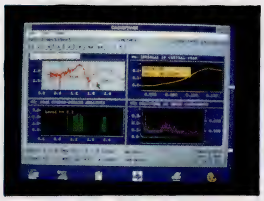

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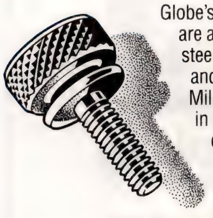

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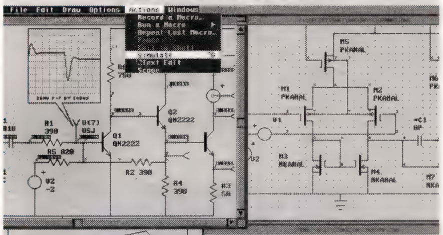

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INTUSOFT CIRCLE 421

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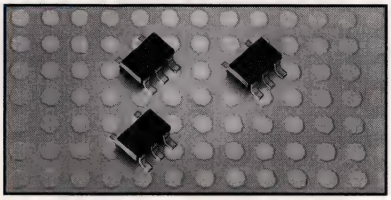

S-807SX high-precision, adjustment-free CMOS voltage detectors provide more precise detection voltage (±2.4%) and half the power consumption (1.0µA typical) of other voltage detectors for longer battery life and more stable switching (5% hysteresis). They feature a wide operating voltage range (1.0-15V), wide operating temperature range (-30° C to +80° C) and two output forms (Nch opendrain and CMOS). Their super miniature SOT-23-5 packages are ideal for cellular phones, hand-held instruments, notebook computers, medical equipment and other advanced applications. TO-92 and SOT-89 package versions are also available.

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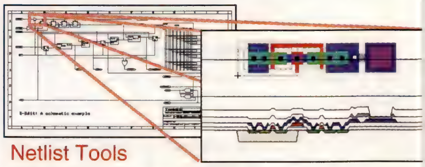

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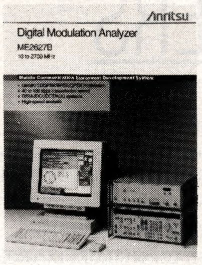
DIGITAL MODULATION ANALYZER DESCRIBED



A six-page, full-color brochure on the ME2627B digital modulation analyzer describes suitable applications for the instrument as well as all its features and specifications. Available screen displays—including spectrum, eye pattern, constellation, phase/frequency error, power error, and modulation error—are pictured. The brochure offers information on analysis parameters, mobile communications systems that can be tested, and circuit component evaluation applications. The publications is available without charge from Anritsu-Wiltron Sales Co., Morgan Hill, Calif. JN **CIRCLE 940**

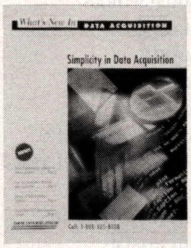
SPICE NEWSLETTER DISCUSSES SIMULATION

Dedicated to discussing topics related to the Spice circuit-simulation tool, the Intusoft Newsletter's most recent issue contains two articles and numerous news items detailing recent developments. The newsletter is produced by Intusoft, San Pedro, Calif. One application note, titled "New Models Simulate PCB Effects," covers various issues surrounding the simulation of pc-board effects such as ground and V_{CC} bounce. Another article describes how to perform a Monte Carlo statistical yield analysis on active filters using the company's FilterMaster Active program and IsSpice. A floppy disk containing all the schematics and Spice models in the newsletter is available for a small fee. Also offered is a yearly subscription to the newsletter. DM **CIRCLE 941**

AP NOTE DISCUSSES OSCILLOSCOPE PROBES

An application note called "Probes and Probing" describes the problems most frequently encountered in probing electronic signals and explains how to choose the right probe for various applications. A probe's dynamic characteristics often have to be matched with those of the logic type being used, so the note, from LeCroy Corp., Chestnut Ridge, N.Y., discusses specific logic families. Also examined are the problems involved with looking at signals on low-impedance transmission lines and the effects of probe grounding. The note contains information on the use of high-impedance probes, low-capacitance probes, and active (FET) probes. Users of both analog and digital oscilloscopes will find the note beneficial. JN **CIRCLE 942**

GUIDES DETAIL DATA, IMAGING PRODUCTS

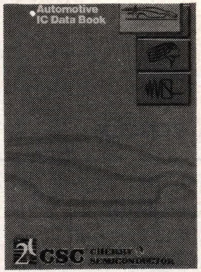

What's New In DATA ACQUISITION
Simplicity in Data Acquisition

Two short-form guides summarize PC AT and VME-bus product offerings, highlighting recent introductions. The eight- and 10-page brochures, available without charge from Data Translation, Marlboro, Mass., are "What's new in data acquisition" and "What's new in imaging." The former describes the company's latest data-acquisition hardware and software and includes a table summarizing their features and those of the rest of the company's data-acquisition and chromatography products. The latter guide details products for imaging and image analysis. Pricing and ordering information are included in the guides. JN **CIRCLE 943**

HOW SETTLING TIME AFFECTS DATA ACCURACY

An application note from National Instruments Corp., Austin, Tex., discusses the inaccuracies that instrumentation amp settling times can cause in data acquisition. "Is Your Data Inaccurate Because of Instrumentation Amplifier Settling Time" defines settling time as the time needed for a signal to reach a certain accuracy and stay within a specified range. The note explains how users can test data acquisition boards to determine the dc and ac settling time of the instrumentation amplifier. It describes how gain, multiplexing, source output impedance, and transition-line resistance and capacitance affect settling time. Two ways to reduce the effects of settling time are also covered. JN **CIRCLE 944**

AUTOMOTIVE ICs IN DETAILED GUIDE



A 264-page guide to ICs for auto applications from Cherry Semiconductor Corp., E. Greenwich, R.I., includes detailed data on regulators, power-supply-control ICs, power-conversion support circuits, motor driver/controller ICs, ignition-driver ICs, solenoid and relay driver ICs, and sensor and multiplexing ICs. Included are handy selection guides for linear regulators and H-bridge drivers as well as complete information on packaging options. Specifications, diagrams, technical drawings, and feature summaries are provided for all products. DM **CIRCLE 945**

DC-DC HANDBOOK CONTAINS ALL SPECS

A comprehensive product handbook contains complete electrical and mechanical specifications on a full line of over 600 dc-dc converters. The 128-page handbook, from Conversion Devices Inc., Brockton, Mass., includes many new products with wide input ranges and high input-to-output isolation, among other features. Also included are 34 pages of application and technical notes with in-depth information on dc-dc-converter topics such as product testing, theory of operation, thermal characteristics, and more. DM **CIRCLE 946**

CATALOG LISTS PC-BASED DEVELOPMENT TEST TOOLS

A 36-page, two-color catalog describes a broad range of PC-based development test instruments from the recently formed Instrument Products Div. of Emulation Technology Inc., Santa Clara, Calif. Included are in-circuit emulators, simulators, programmers, and logic analyzers, as well as related software and accessories. A solutions section discusses potential problems in project development and how the listed tools can solve those problems. Also in this section is a set of recommended PC configurations for each product, listing requirements such as memory and speed. JN **CIRCLE 947**

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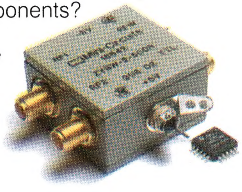

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